TOT measurement implemented in FPGA TDC [*]

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Abstract: Time measurement plays a crucial role for the purpose of particle identification in high energy physics experiments. With increasingly demanding physics goals and the development of electronics, modern time measurement systems need to meet the requirement of excellent resolution specification as well as high integrity. Based on Field Programmable Gate Arrays (FPGAs), FPGA time-to-digital converters (TDCs) have become one of the most mature and prominent time measurement methods in recent years. For correcting the time-walk effect caused by leading timing, a time-over-threshold (TOT) measurement should be added to the FPGA TDC. TOT can be obtained by measuring the interval between the signal leading and trailing edges. Unfortunately, a traditional TDC can recognize only one kind of signal edge, the leading or the trailing. Generally, to measure the interval, two TDC channels need to be used at the same time, one for leading, the other for trailing. However, this method unavoidably increases the amount of FPGA resources used and reduces the TDC's integrity.

This paper presents one method of TOT measurement implemented in a Xilinx Virtex-5 FPGA. In this method, TOT measurement can be achieved using only one TDC input channel. The consumed resources and time resolution can both be guaranteed. Testing shows that this TDC can achieve resolution better than 15ps for leading edge measurement and 37 ps for TOT measurement. Furthermore, the TDC measurement dead time is about two clock cycles, which makes it good for applications with higher physics event rates.

Key words: time-over-threshold (TOT) measurement, field programmable gate array (FPGA), time-to-digital converter (TDC)

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1   Introduction

Time measurement plays a crucial role for particle identification in high energy physical experiments, especially in time-of-flight (TOF) detectors [1–3]. Dedicated TDC ASICs or FPGA TDCs can both be used to implement time measurement. Compared with ASIC TDCs (e.g. HPTDC [4]), the FPGA TDC [5–9] has the advantages of shorter development time, higher flexibility and lower cost. FPGA TDC techniques have developed rapidly in recent years.

For precise time measurements, the technique of signal timing should be considered seriously. Various kinds of timing methodology have been widely developed, such as leading edge timing (LET), constant fraction timing (CFT) etc. [10–12]. Compared with CFT, the structure of LET is very simple. LET only consists of a comparator and several passive elements, which has made it one of the most popular technologies for timing. A mark indicating the event time is generated by LET once the signal reaches the threshold. However, this timing mark inevitably depends on the signal amplitude. This is the time walk phenomenon. It restricts the LET timing precision, brings time measurement errors and deteriorates the time resolution. Fortunately this error can be corrected by the signal charge information [13].

Traditionally, two independent circuits should be used to measure the time and charge respectively. For simplification, a dedicated TDC ASIC is used to measure the time. The charge measurement circuit, however, can only be implemented by discrete components, which make the circuit very complex.

Electronics for high energy physics experiments are increasingly high resolution and high density. For example, the number of electronic channels in the BESIII end-cap time-of-flight (ETOF) system will increase to 1728 after it is upgraded - this is an almost twenty-fold increase. It is crucial and urgent to simplify the ETOF electronic system structure and increase its integrity for the upgrade.
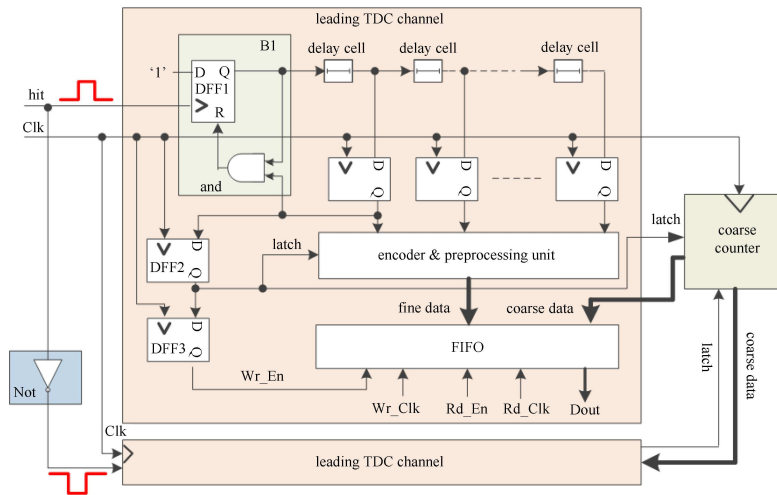
Fig. 1.   (color online) Block diagram of pulse width measurement with two TDC channels.

Recently, many dedicated leading edge discriminators (LEDs) based on a time-over-threshold approach, such as NINO and PADI [14–16], have been developed for time measurement. The rising edge of the discriminator output represents the hit signal time information, while the pulse width represents the charge amount. Devices with the capability of measuring time and pulse width simultaneously can simplify TDC measurement circuits greatly.

In our previous work [8], a high resolution TDC has been implemented in a Xilinx FPGA. It applies the methodology of combining coarse and fine time measurement. Coarse time measurement utilizes a normal binary counter to measure coarse time, which is a multiple of the clock period. The fine time, less than one clock period, is measured by fine time measurement. It utilizes dedicated carry chain resources in the FPGA to construct a delay chain for time interpolation. The TDC time measure precision with this structure can be better than 15 ps. By reversing the input signal and measuring its trailing edge, the pulse width can easily be measured and the resolution can reach about 27 ps. The TDC structure is shown in Fig. 1. Obviously, to measure the pulse width, two independent input channels should be used, one for the leading edge measuring and another for the trailing edge. This means that TDC integrity decreases and the cost increases.

A high resolution and high density method of TOT measurement is proposed in this paper. It is implemented and evaluated on a Xilinx Virtex-5 FPGA. The time and pulse width can be obtained simultaneously in one channel with this method.

2   Implementation of TOT measurement

The simplest way of measuring pulse width is to obt-

ain the leading and trailing edge times and subtract them to obtain the pulse width. The leading edge time can be obtained by the TDC shown in Fig. 1, so the goal is to find a way to obtain the trailing edge time in the same TDC channel.

2.1   Slice structure of Virtex-5 FPGA

As shown in Fig. 2, every slice in the Virtex-5 FPGA [17] contains four LUTs (Look-Up Tables), four DFFs (D Flip-Flops) and a dedicated fast carry chain called CARRY4 Primitive. The carry chain runs upwards and has a height of four bits per slice. For each bit, there is a carry multiplexer (MUXCY) and a dedicated XOR gate as shown in the red circles in Fig. 3. The outputs (COi, Oi) can be stored in a DFF controlled by a multiplexer.
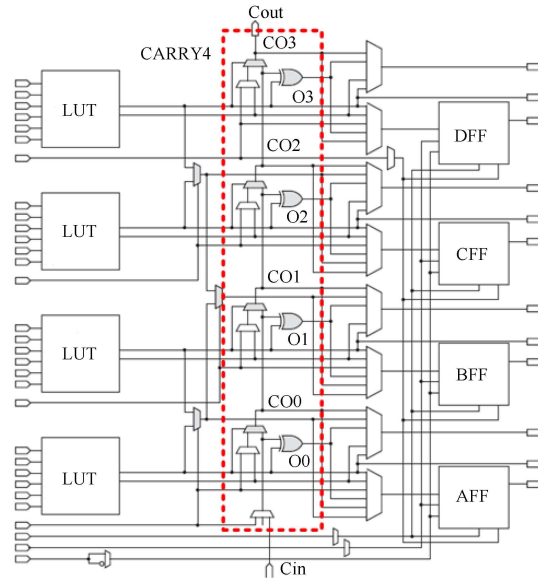

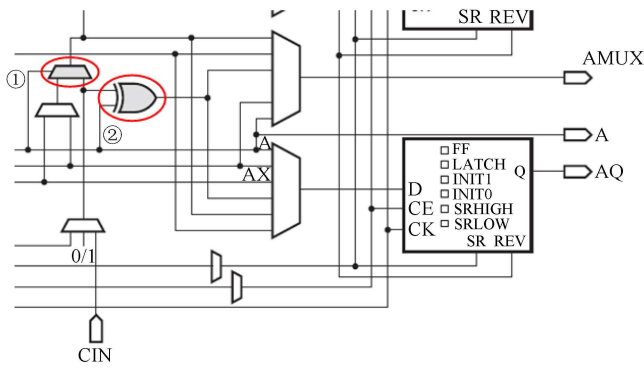Fig. 2.   (color online) Structure of slice resources in Xilinx Virtex-5 FPGA.

Fig. 3.   (color online) Enlarged drawing of the first bit of the slice.

To construct a delay cell with this carry chain, all the MUXCYs select Cin as the input channel. The select port of the MUXCYs, marked '①' in Fig. 3, must be set to '1'. This sets one input of the XOR gate, marked '②' in Fig. 3, to '1'. When a signal with a rising edge passes through this carry chain, the output, CO0, CO1, CO2 or CO3, of the MUXCYs changes from '0' to '1'. Similarly, when a signal with falling edge comes, the output, O0, O1, O2 or O3, of the XOR gates also changes from '0' to '1'. So the MUXCY can be used to detect the rising edge and the XOR gate can be used to detect the falling edge.

2.2   Implementation

The block diagram of a new TDC with this method is shown in Fig. 4. The 'Hit' signal is fed into the carry chain, which is comprised of CARRY4 Primitives. In each CARRY4 Primitive, taps from the ports 'CO0' and 'CO3' are drawn to construct delay cells for leading edge time measurement and a tap from 'O2' is for trailing edge time measurement. The tap status, presenting the 'Hit' signal fine time measurement, is stored in the DFFs at each clock rising edge. The time is encoded in the Encoder and Processing Unit once a true 'Hit' signal occurs. The encoder unit is shared by the leading edge time measurement and trailing edge time measurement. Finally, fine and coarse data representing the leading and trailing edge respectively are written into the same FIFO. Data for the different edges is signed by some specified bits.

The TDC performance can be greatly degraded by differential non-linearity (DNL) and integral non-linearity (INL). The larger the DNL and INL are, the worse the TDC resolution becomes.   Non-linearity is mainly caused by the non-uniformity of the delay cells and imperfect clock distribution to FPGA registers. As shown in Fig. 2, there is a multiplexer at the beginning of the CARRY4 Primitive. This is called the Asymmetric Factor (AF) [8]. It makes the four bits' delay time in the CARRY4 Primitive unequal. To make the delay cells as uniform as possible to maximize improving the TDC resolution, taps from the port 'CO0' and 'CO3' are taken for the leading edge measurement [8]. Because the remaining two bits in the middle cannot averagely subdivide one slice, only the tap from port 'O2' is taken for the trailing edge time measurement. This means that the whole slice or CARRY4 Primitive acts as a single cell to construct the delay chain for trailing edge measurement.
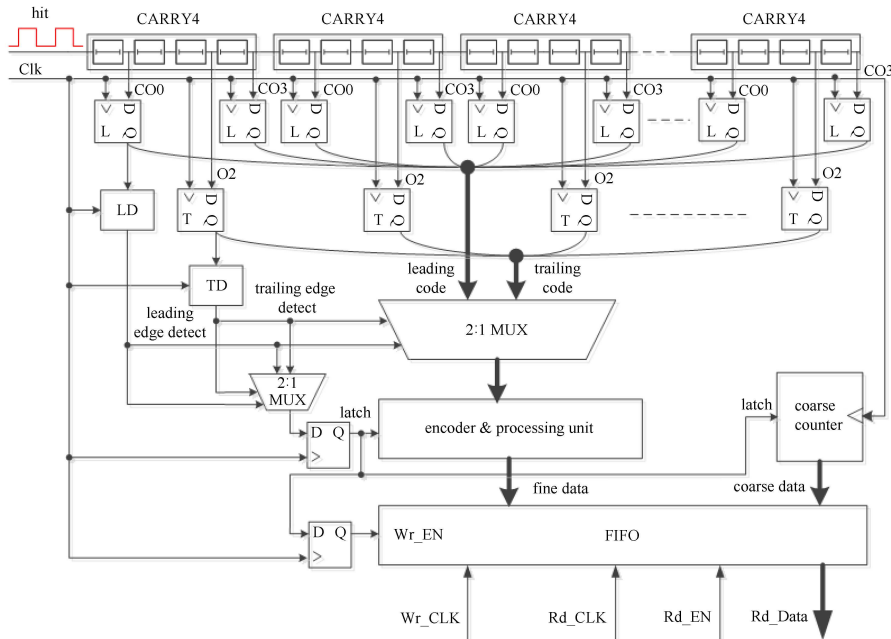

Fig. 4.   (color online) Architecture of time digitizing system for ETOF upgrade.

Because the encoder unit is shared by the leading and trailing edge time measurement, to identify the edges and indicate the signal validity, two detecting units, LD (Leading edge Detect) and TD (Trailing edge Detect), are inserted into the first delay cells respectively, as shown in Fig. 4. Besides, the two detecting units can also be used to decide when and which edge's code should be sent to the encoder unit for encoding.

The output of the LD or TD controls one 2:1 multiplexer to decide which edge code should be encoded, and is also sent to another 2:1 multiplexer to latch the encoder result and enable the FIFO writing operation after being delayed. The specific circuit and timing diagram of the detect unit is shown in Fig. 5. It uses a NOT gate, a DFF and an AND gate to generate a pulse with one clock width when a rising edge comes.
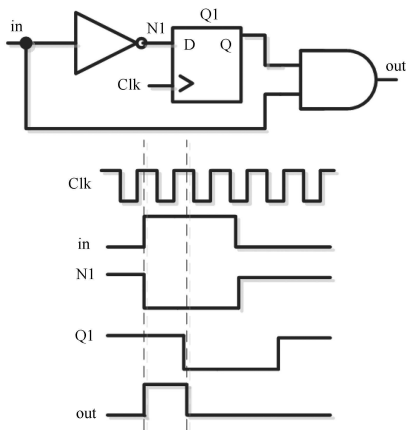

Fig. 5.   The specific circuit and timing diagram of the hit signal detect unit.

2.3   Dead time

Since the encoder is based on the dichotomizing search principle, the TDC code is thermometer code ($000\cdots0111\cdots1$) and the position of the edge can be determined at the '0-1' transitions. To make the outputs of the registers be thermometer code, the high and low level of the 'Hit' signal must both be at least one clock width. The smallest interval of two adjacent leading edges must

be larger than two clock periods, so the TDC's dead time in measuring the leading edge is at least two clock periods. Because one leading edge can be encoded during two clock periods, the following leading edge can be latched into the registers successfully if it comes after two clocks. Because the encoding process does not increase the dead time, the TDC's total dead time is two clock cycles.

3   Experiments

A 6U VME evaluation board with a Xilinx Virtex-5 FPGA (XC5VLX220FF1760) has been designed. There are two TDC channels on it. The system clock frequency of the TDC is 250 MHz. The layout of one slice is shown in Fig. 6. The blue lines represent the programmed lines. The bits of CO0, CO3 and O2 are successfully routed and distributed to the related delay chains.
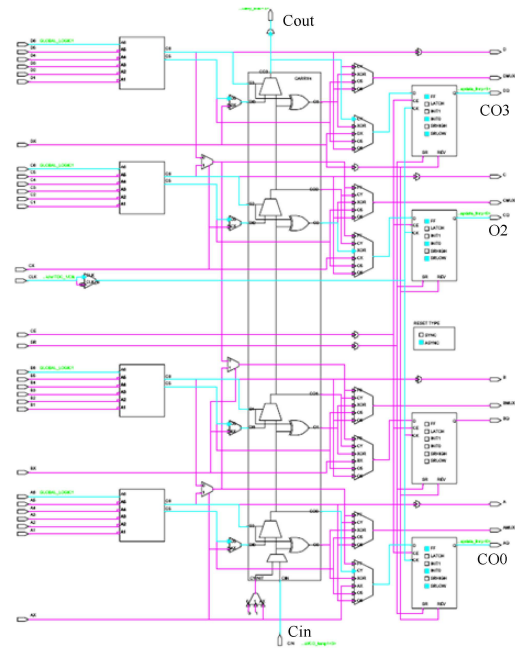

Fig. 6.   (color online) Layout of one slice of the pulse width measurement.
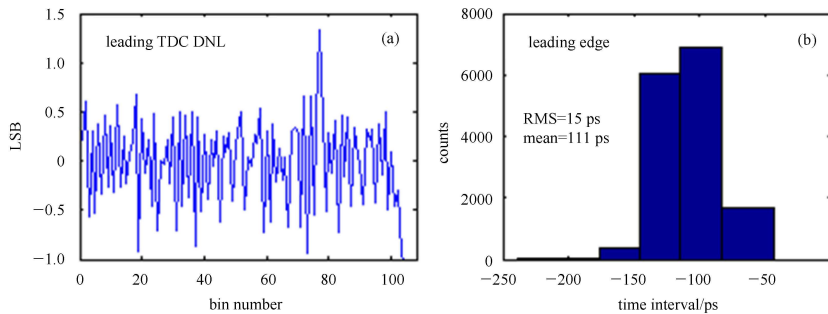

Fig. 7.   (a) DNL feature of leading TDC; (b) Time resolution of leading TDC.
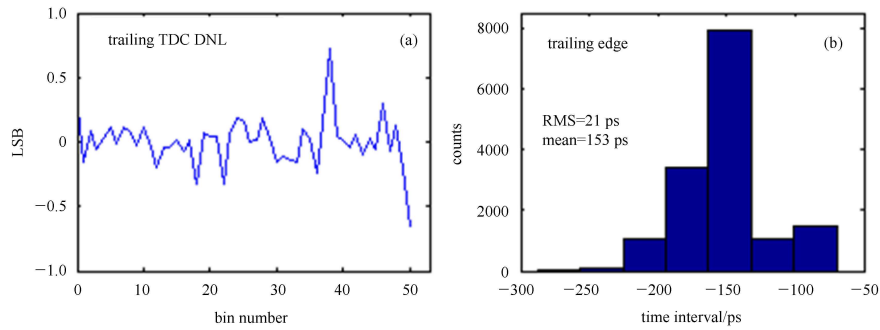
Fig. 8.   (a) DNL feature of trailing TDC; (b) Time resolution of trailing TDC.
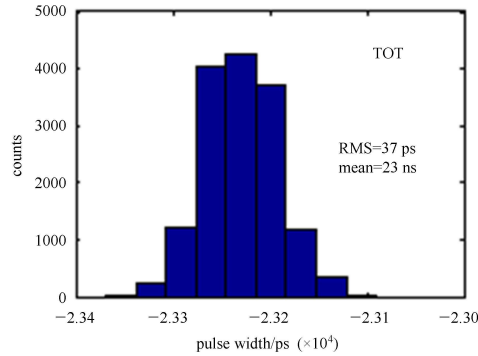

Fig. 9.   (color online) Resolution of pulse width measurement with one TDC channel.

The cable delay method [18, 19] is applied to evaluate the TDC's time measurement resolution. The DNL features of the leading and trailing TDC are shown in Fig. 7(a) and Fig. 8(a) respectively. The bin numbers are 105 and 51 respectively. The LSB for the leading TDC is about 38ps and for the trailing is about 78 ps. As expected, the trailing TDC's LSB is almost twice that of the leading TDC's. Besides, there are some large values in both of the two TDCs' DNLs. This is caused by the structure of the Xilinx FPGA.

The resolution of the leading and the trailing edge measurement is about 15 ps (Fig. 7(b)) and 21 ps (Fig. 8(b)) respectively. Although the trailing edge resolution is worse than that of the leading edge, it is enough for Time-Walk correction in most high energy physics experiment applications.

One hit signal with 23 ns pulse width is fed into one TDC channel. Figure 9 shows that the resolution of the pulse width measurement is about 37 ps.

4   Conclusions

In this paper, a method of measuring pulse width implemented in a Xilinx FPGA is proposed. This method implements time and pulse width measurement simultaneously in one TDC channel. This greatly improves the TDC integrity and reduces the whole cost. Test results show that the performance of this TDC is: (1) leading edge time measurement resolution: ∼15 ps; (2) trailing edge time measurement resolution: ∼21 ps; (3) pulse width measurement resolution: ∼37 ps; (4) dead time: ∼10 ns.

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