A prototype silicon detector system for space cosmic-ray charge measurement

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Abstract: A readout electronics system used for space cosmic-ray charge measurement for multi-channel silicon detectors is introduced in this paper, including performance measurements. A 64-channel charge sensitive ASIC (VA140) from the IDEAS company is used. With its features of low power consumption, low noise, large dynamic range, and high integration, it can be used in future particle detecting experiments based on silicon detectors.

Key words: VA140, ASIC, readout electronics, silicon detector, charge measurement

PACS: 07.05.Hd **DOI:** 10.1088/1674-1137/38/6/066101

1 Introduction

With the development of semiconductor technology, fully-depleted silicon detectors have become widely used in particle physics, medical instruments, and astrophysics because of their low noise, high counting rate, and good linearity. In the field of space astrophysics detection, they are used by many experiments to measure the charge of ionizing particles. The energy loss from a heavy charged particle passing through a given thickness of fully-depleted silicon detector is due to ionization. The mean energy loss is proportional to Z^2, according to the Bethe-Bloch formula. Accurate mean energy loss measurements by silicon detectors can, therefore, be used in the identification of cosmic nuclei.

A typical readout electronics system for charge measurement consists of a charge sensitive preamplifier, shaper, peak holder, A/D converter, and control circuit. The large area silicon detectors used in space cosmic-ray charge measurement, such as silicon matrix detectors, silicon pixel detectors, and silicon micro-strip detectors, often contain thousands of readout channels. Detectors with a large number of readout channels face great challenges in space missions. Integration, reliability, and power dissipation would be extremely complicated if traditional discrete transistors, diodes and amplifiers are chosen for readout electronics. Given that the allowed power, weight and volume are very limited on board satellite platforms, Application Specific Integrated Circuits (ASICs), which have low noise, low power, and high integration, are frequently used in the readout electronics for multi-channel silicon detectors in the space exploration area [1]. In the Advanced Thin Ionization Calorimeter experiment (ATIC, 1999), the silicon matrix consists of 4480 Si-PIN detectors that are read out using 16-channel ASICs (CR-1) [2]. In the Alpha Magnetic Spectrometer 02 experiment (AMS-02, 2011), the silicon tracker contains a total of 196,000 silicon strip channels, which are read out by 64-channel ASICs (VA64HDR9A) [3].

In this paper, a prototype readout electronics system for a silicon detector based on the ASIC VA140 is introduced.

2 Overview of VA140

The VA140 is a 64-channel, low noise, low power and +/−200 fC high dynamic range charge measurement ASIC designed by IDEADS (Norway). As shown in Fig. 1, each readout channel consists of a charge sensitive preamplifier, a shaper, and a sample/hold circuit. An analogue multiplexer controlled by a shift register is adopted to shift all of the holding signals of the 64 channels to a common differential output. In addition, it has calibration facilities which enable the linearity of each channel to be calibrated by an external charge injection [4].

Received 11 July 2013, Revised 3 December 2013

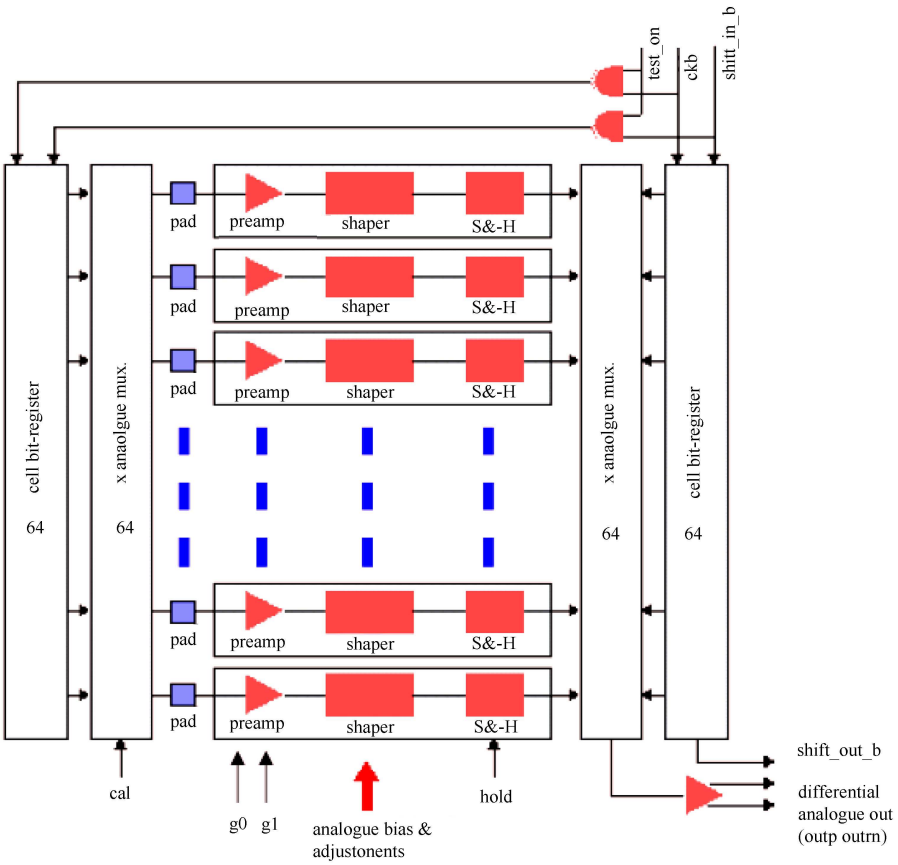

Fig. 1. VA140 internal architecture.

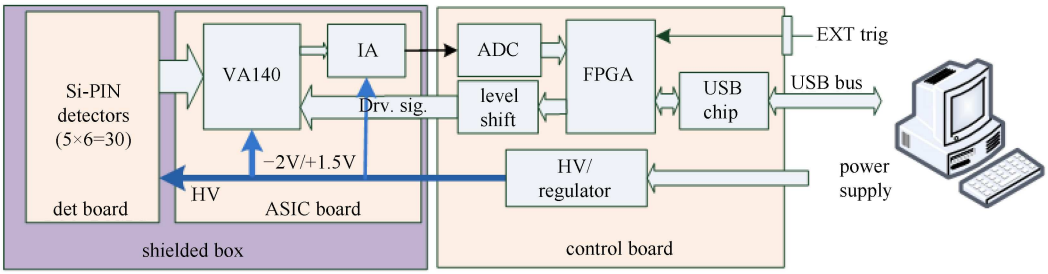

Fig. 2. Readout electronics block diagram.

3 Hardware for readout electronics

As shown in Fig. 2, the readout electronics block diagram consists of three boards: a control board, an ASIC board, and a detector board. A shielded box is used to prevent external light and EMI from interfering with the silicon detectors and ASIC. On receipt of an external event trigger, the control board will drive the VA140, digitize signals, and transfer data to the PC.

3.1 Control Board

The control board is responsible for controlling the VA140, digitizing analog signals, and transferring data packets to a PC through a USB port. It contains a power generator module for both high and low voltage power, a controlling FPGA (XC3S500E), a 14-bit 3MSPS ADC (AD9243), and a USB interface chip (CY7C68013). A level shift circuit due to the mismatched voltage levels between the FPGA and VA140 is used to convert the FPGA driver level from 0–3.3 V to −2 V–+1.5 V. An HV module (E10222 from EMCO company) is used to generate the 80 V bias voltage for the detector.

3.2 ASIC board

The ASIC VA140 is put in the ASIC board. It receives the driver signals from the control board and sam-

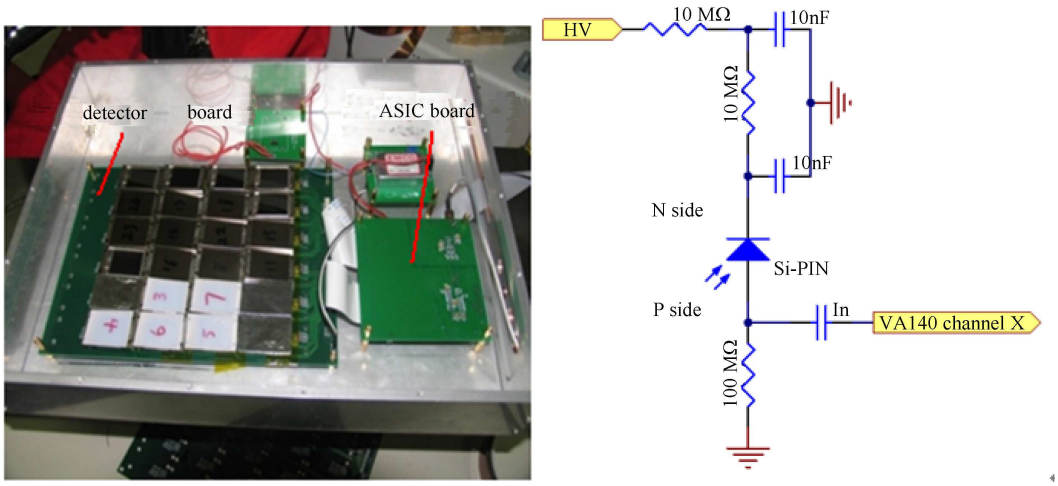

Fig. 3. Frontend electronics of Si-PIN detector.

ples charge signals from the front detectors. An instrumentation amplifier circuit is used to convert the differential output signal of VA140 to a single-ended signal.

3.3 Detector board

There are 24 Si-PIN detectors mounted on the detector board. The area and thickness of each detector are 5 cm^2 and 300 μm, respectively. The detectors are connected to the VA140 channels (ch-1 to ch-24) separately through flexible cables. The frontend circuit schematic for each Si-PIN detector is shown in Fig. 3. Two 10 MΩ resistors and two 10 nF capacitors near the detector are adopted to filter the HV bias. When a charged particle or a high-energy photon goes into, or through, the fully-depleted area of the detector, electrons and holes will be generated and travel to the N side or P side, respectively. A 100 MΩ resistor is used to sample the positive signal on the P side, and the charge is injected to the preamplifier of a certain VA140 channel through a 1 nF coupling capacitor.

4 Software of the readout electronics

The software for the readout electronics includes a logic program in the FPGA and application software on the PC.

The FPGA logic is designed using the High Speed Integrated Circuit Hardware Description Language (VHDL) and synthesized with the Xilinx ISE tools. As shown in Fig. 4, during normal operation, the FPGA receives configuration commands from the PC through the USB bus, then drives the operation of the VA140 and ADC, and transfers the data to the PC. An internal 8K×16 bits FIFO inside the FPGA is used to buffer the event data.

The readout timing of the VA140 is shown in Fig. 5. When an event happens the VA_Driver module in FPGA will give the [holdb] signal after a fixed 6.5 μs delay in order to hold the shaper signals for all channels. The FPGA will then give the [shift_inb] and [ckb] signals to trigger the VA140 to shift out the sampling analog signals channel by channel. The ADC will digitize the signals at the same time. Since the shift clock [ckb] frequency is 1 MHz, it will take 64 μs to read all the 64 channels for one external event trigger.

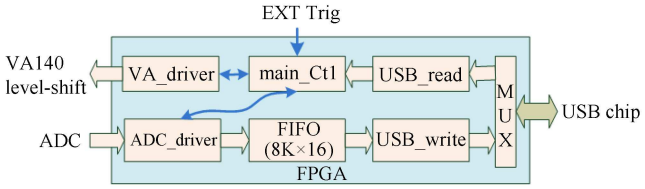

Fig. 4. Logic block diagram in the FPGA.

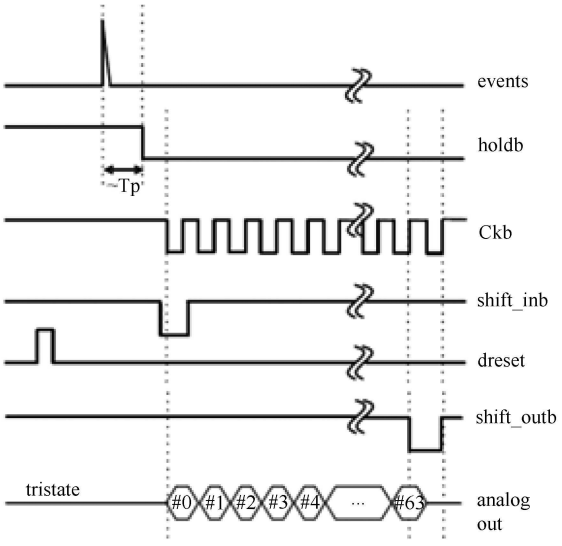

Fig. 5. Readout timing of the VA140.

The PC application is developed in C and is based on Labwindows/CVI, as shown in Fig. 6. It provides a user-friendly Graphical User Interface (GUI) by means of which we can configure the parameters of the readout electronics, read data packets through the USB bus, process and display online.

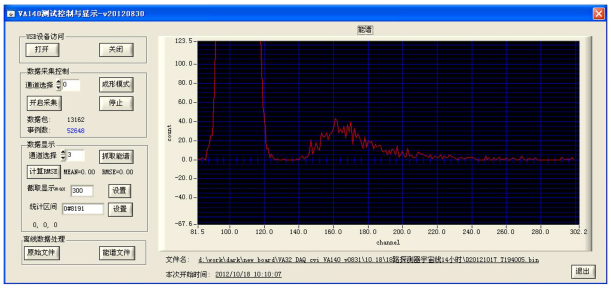

Fig. 6. PC software based on Labwindows/CVI.

5 Performance tests

5.1 Power dissipation

The readout electronics are powered by external +5 V and −5 V DC modules whose currents are 130 mA and 40 mA, respectively, under normal operations. For the −2 V and +1.5 V VA140 power supply generated from the external −5 V and +5 V through low-dropout voltage regulators, the currents are about 8 mA and 2 mA, respectively. The power dissipation for each channel is around 0.3 mW.

5.2 Integral nonlinearity test for VA140

The VA140 input charge from the silicon detectors can be simulated by a pulse voltage going through a capacitor. The value of the charge is equal to the result of multiplying the pulse amplitude by the coupling capacitance. In order to measure the linearity of the VA140, a serial of pulses with increasing amplitudes from 10 mV to 200 mV are generated by a DG4162 signal generator. A 2 pF coupling capacitance is connected to the VA140 input channel 1. The linearity curve of VA140 is shown in Fig. 7, with the integral nonlinearity (INL) being better than 3% in the 0 to 200 fC range.

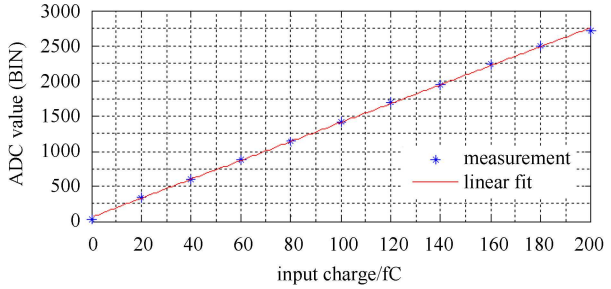

Fig. 7. Linearity curve of the VA140.

5.3 Noise slope test with different input capacitors

To simulate the capacitive load of the detectors, various capacitors (0 pF to 510 pF) were mounted between the ground and input channel 1. The noise slope is shown in Fig. 8, and is approximately 0.0018 fC/pF (i.e. 11 e/pF).

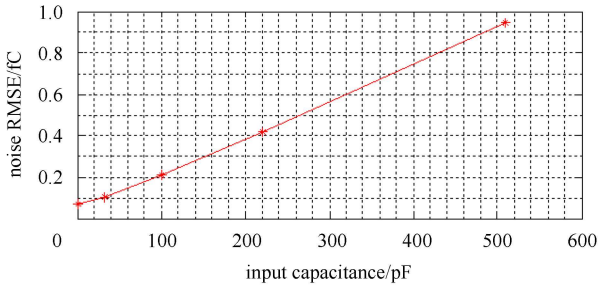

Fig. 8. Noise slope curve of the VA140.

5.4 Pedestal and noise test

VA140 input channels 1 to 24 were connected to the Si-PIN detectors, while the remaining channels were not connected. The pedestal and noise were tested with a 100 Hz random trigger. As shown in Fig. 9, the noise values (RMSE) of the channels, both with and without the detectors connected, are about 0.35 fC and 0.07 fC,

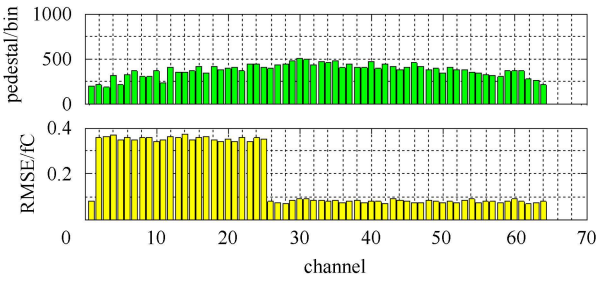

Fig. 9. Pedestal and noise test for the VA140.

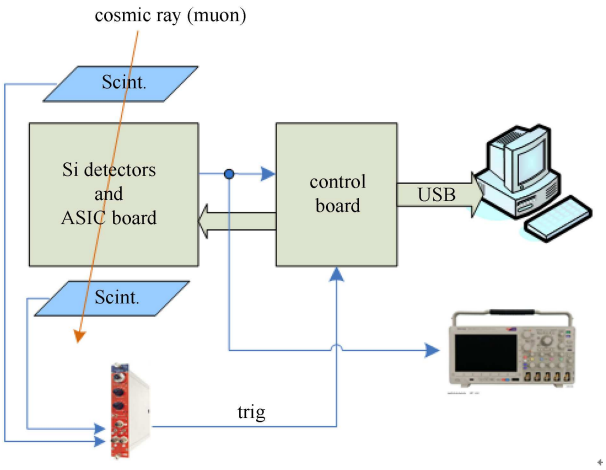

Fig. 10. Cosmic ray test system in the laboratory.

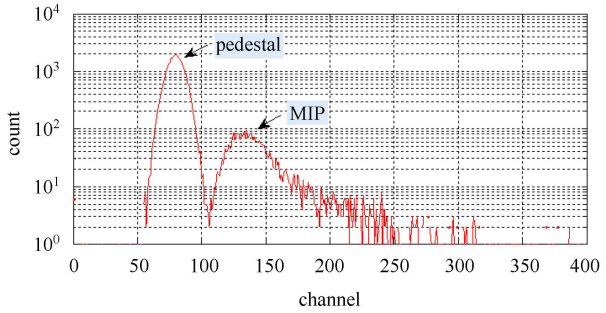

Fig. 11. MIP curve of cosmic rays (muons).

respectively. The increased noise with the detectors connected is due to the capacitance and leak current of the detectors.

5.5 Cosmic ray test

In order to test the detector performance for Minimum Ionizing Particles (MIPs), a cosmic ray (muon) test system was set up in the laboratory. As shown in Fig. 10, two scintillators on and underneath the silicon detectors were used to generate a coincidence trigger when a muon particle went through the detectors. The control board read all the VA140 channels and sent the data to the PC with every trigger.

The cosmic ray test system worked stably in a continuous 48 hour test. The cumulative energy spectrum is shown in Fig. 11. The MIP spectrum of muons obeys a Landau distribution and can be clearly distinguished from the pedestal.

6 Conclusion

A readout electronics system for silicon detectors for space cosmic-ray charge measurement is presented in this paper. The readout electronics have low noise (less than 0.1 fC with the silicon detectors connected), low power dissipation (about 0.3 mW/channel), high dynamic range (200 fC), and high integration (64 channels in one chip). Such a system can be used in many future space particle detection experiments.

The authors would like to thank the DAMPE project of the Chinese Strategic Priority Research Program in Space Science for their support.

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