R&D of an LLRF control system for a 162.5 MHz radio frequency system

WEN Liang-Hua(文良华)[1,2] WANG Xian-Wu(王贤武)[1] HE Yuan(何源)[1] CHANG Wei(常玮)[1,3]
ZHANG Rui-Feng(张瑞峰)[1] ZHANG Sheng-Hu(张生虎)[1] ZHU Zheng-Long(朱正龙)[1]
LI Chun-Long(李春龙)[1] SHI Long-Bo(施龙波)[1] ZHANG Rui(张锐)[1]

[1] Institute of Modern Physics, Chinese Academy of Sciences, Lanzhou 730000, China
[2] School of Physics and Electronic Engineering, Yibin University, Sichuan 644000,China
[3] University of Chinese Academy of Sciences, Beijing 100049, China

Abstract: This paper describes a low level radio frequency control system that was developed by the Institute of Modern Physics Chinese Academy of Sciences, and will be used in Injector Ⅱ of the China-ADS project. The LLRF control system consists of an RF modulated front end, fast analog-to-digital converter (ADC) modules, and a digital signal processing board based on a field programmable gate array. The system has been tested on a room temperature cavity with 12-hr, and the results illustrate that the stability of amplitude and phase achieved ±0.32% and ±0.35 degrees, respectively.

Key words: LLRF, resonance, amplitude, phase, stability

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1 Introduction

One of the superconducting cavities developed by the Institute of Modern Physics Chinese Academy of Sciences (IMPCAS) is a 162.5 MHz, half-wave resonator. To control the resonant frequency and regulate the amplitude and phase of the cavity, a Low Level Radio Frequency (LLRF) control system has been developed to achieve a field amplitude stability of ±0.5%, a phase stability of ±0.5°, and a cavity tuning phase error of ±0.6°. The functions of the LLRF system are implemented by using digital control loops based on phase, amplitude, and quadrature demodulation techniques. A block diagram of the LLRF system is shown in Fig. 1. In most LLRF control systems operated in LABs, the control loop is directly based on I/Q, which adopts a complicated average algorithm for amplitude and phase stability control; the tuner controller was partly implemented. The analysis and measurement between system clock jitter and the stability of phase and amplitude is

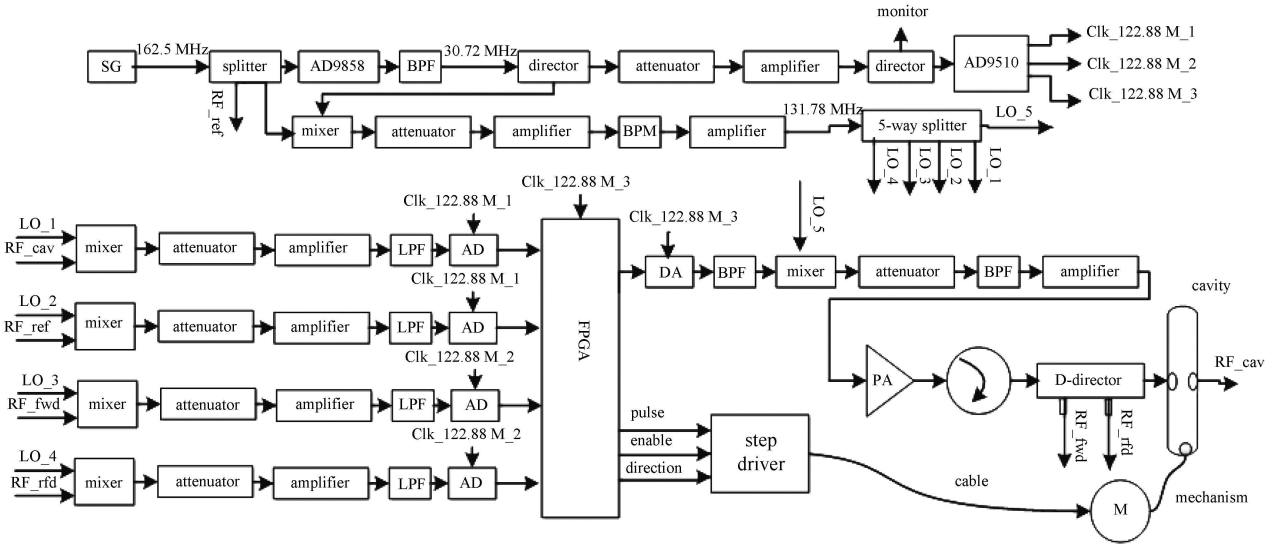

Fig. 1. The schematic of LLRF control system for 162.5 MHz radio frequency system.

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rarely mentioned. To improve the system performance and verify the control algorithm, a control loop based on an amplitude and phase, I/Q CIC average filter, the effect of clock jitter, a tuner control integrated in the stability controller, and loop parameter tests were carried out for development of the LLRF system.

The prototype LLRF system is composed of two layers of hardware (Fig. 2). The bottom layer contains the power supply module, an AD9858 direct digital synthesizer board, an AD9510 clock distribution board, an ADC sample daughter board, and a digital signal processing FPGA board. The top layer is an RF modulated front end composed of commercial components.

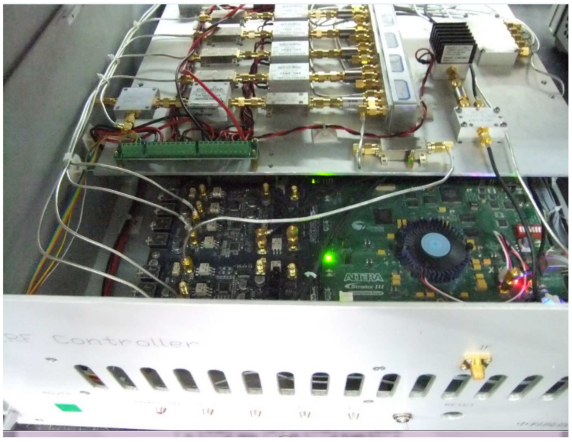

Fig. 2. The layers of the LLRF control system.

2 The clock and jitter

The clock generation and distribution diagram of the LLRF system is shown as Fig. 1. Due to the utilization of quadrature sampling techniques, the clock jitter is critical [1].There are many factors and components which may cause jitter, such as the ripple of power supply, charge pump, low pass filter, and the voltage-controlled crystal oscillator of the phase locked loop (PLL) [2–4]. The total clock jitter is 24.56 ps peak to peak，and the rms jitter is 2.6 ps, as measured by an Agilent DSO9254A oscilloscope. The jitter of the system clock causes less than 0.1° phase error, and meets the phase requirements of the LLRF system.

3 Algorithms in the FPGA

All digital signal processing and loop control algorithms of this LLRF are implemented in a Stratix III FPGA signal processing platform, which consists of a high performance Stratix III EP3SL150F1152 FPGA, two data conversion high speed mezzanine cards with four channels of 150MSPS, 14bits ADCs and four channels of 250MSPS digital to analog converters, and a Marvell 88e1111 device used for 10/100/1000 base-T Ethernet connection [5].

To acquire the phase and amplitude of intermediate frequency (IF) signals, the four output data of ADCs are synchronously in-phase, and quadrature (I/Q) detected, cascaded-integrator-comb filter (CIC) filtered, and CORDIC calculated in the FPGA. The phase and amplitude stability loops are implemented with proportional-integral (PI) control by the digital adjusting phase word of NCO and the digital modulating amplitude of NCO. The tuner controller is supplied with three digital signals (pulse, direction and enable) for the step motor. These signals are generated by a real-time algorithm which calculates the phase error between the reference and actual phase difference of the cavity forward RF power signal and the reflection power signal from the fundamental power coupler. The signal processing flow chart is shown as Fig. 3.

3.1 I/Q detection with DC-filter

In the LLRF system, the frequency of the ADC's clock (122.88 MHz) is four times the IF signal frequency

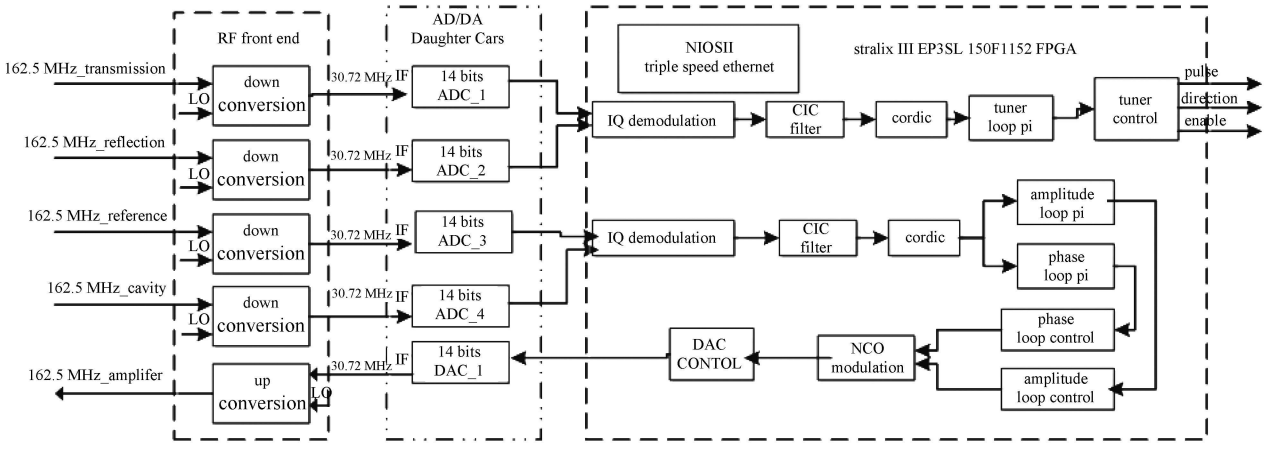

Fig. 3. The digital signal parallel processing flow chart in the FPGA.

(30.72 MHz), locked to each other by a PLL, and embedded in high performance AD9510 chips. So the discrete sequence of IF signal converted by ADCs is

$$A\sin\left(\frac{\pi n}{2}+\phi\right)(n=0,\ 1,\ 2,\ 3\cdots)$$

that is periodic sequence, which is Q, I, $-Q$, $-I$ in a period indicated as in Fig. 4. Using a synchronous I/Q demodulation technique substantially reduces the required logic resources of the FPGA. The formula used for I/Q detection is described below. In addition, the Z transform of the formula (5 or 6) is a DC-filter system function. The frequency response of the DC-filter is shown in Fig. 5. The depression of DC component caused by ADCs is more than 40 dB by this DC-filter.

$$s(n) = A\sin(2\pi f_{\rm IF}nT+\varphi)=A\sin\left(2\pi\frac{f_{\rm IF}}{f_{\rm s}}n+\phi\right)$$

$$= A\sin\left(\frac{\pi n}{2}+\phi\right), \tag{1}$$

$$Q = \frac{s(0)-s(2)}{2}, \tag{2}$$

$$I = \frac{s(1)-s(3)}{2}, \tag{3}$$

$$H(z) = \frac{1-z^{-2}}{2}. \tag{4}$$

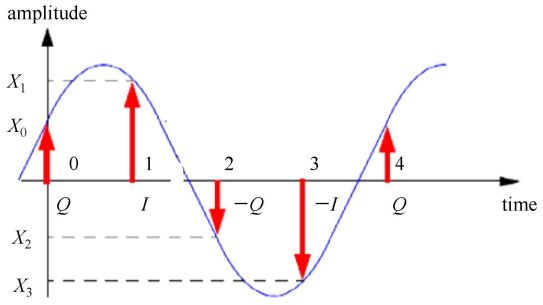

Fig. 4. The IF signal quadrature sample sequence.

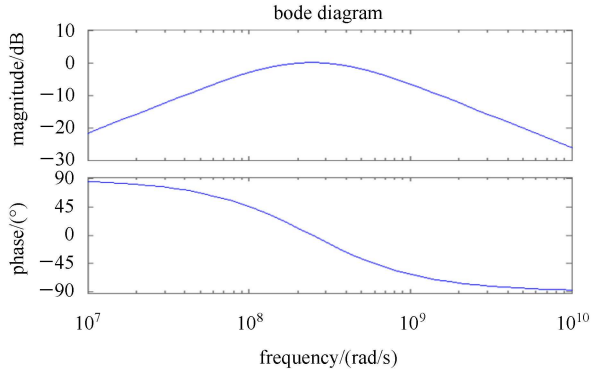

Fig. 5. The Bode plot of the DC-filter.

3.2 CIC average filer

A single stage CIC filter as an average filter was selected for this application and implemented in the FPGA. Such a filter is widely used in sample rate conversion designs, such as digital down-converters and digital up-converters. Here the CIC filter's decimation rate change factor is 128.

$$H_{\rm CIC}(z)=\frac{1-z^{-128}}{1-z^{-1}}. \tag{5}$$

In this CIC filter algorithm, iterative additions (integration) are implemented in 128 clock periods. Then the difference between the last integration result and the current is the averaged output at a rate of one per 128 clock interval. By using this technique for the CIC filter, the singular value of I/Q can be replaced by the nearest I/Q average value. This is shown in Fig. 6, the raw I/Q polar plot ($-\pi$ to π) is a blue curve, and the averaged I/Q polar plot is a red curve.

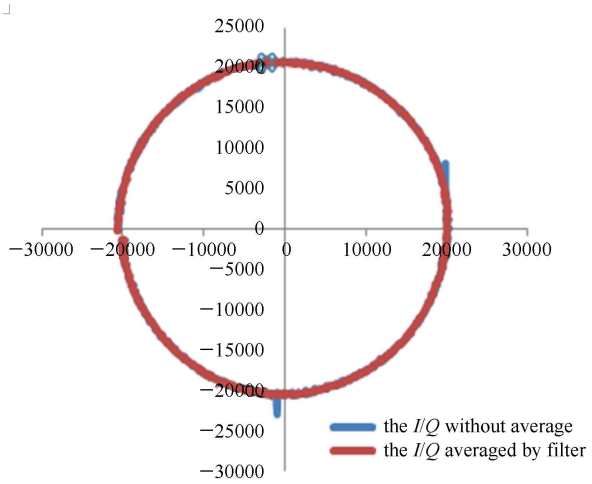

Fig. 6. (color online) The I/Q average effect under I/Q coordination.

4 Test of the system

Due to the excessive cost of testing a real superconducting cavity, the initial test is performed using a room temperature cavity. The system requirements are shown in Table 1. An RF Lock-In Amplifier SR844 developed by Stanford Research System [6] and a power meter N1914A are integrated into the test a the amplitude and phase stability. To analyze the LLRF performance varying with temperature, a Pt. thermal resistor is mounted on the cavity and connected with a multi-function meter to measure the ambient temperature. They are used to validate the temperature stability of the LLRF system over a limited range. Because the tuner was not implemented, only the amplitude and phase stability measurements have been validated during this room temperature test.

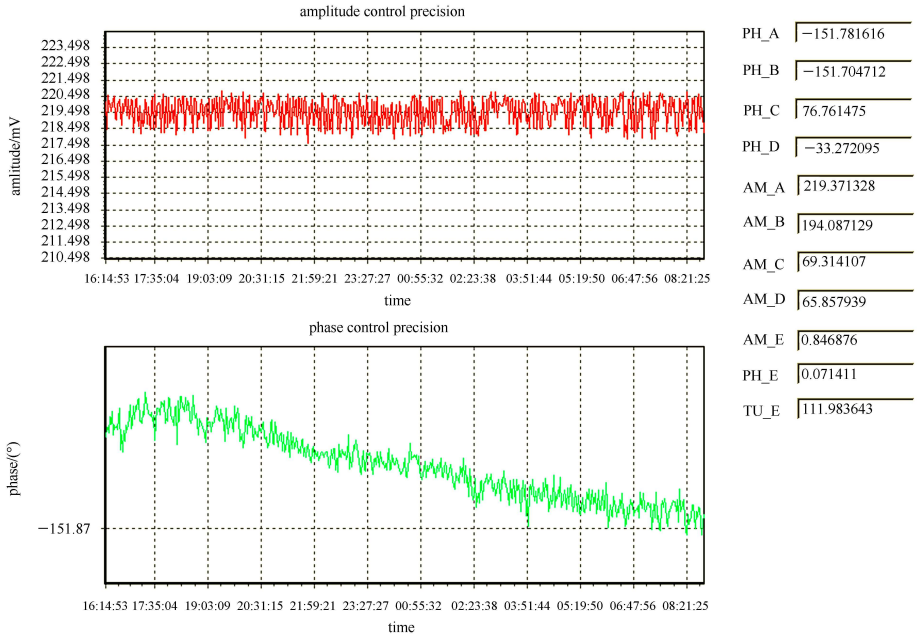

Fig. 7. The LLRF twelve-hour amplitude and phase stability test result.

Table 1. The requirements of the LLRF system.

specification	test	target
resonant frequency f/MHz	162.9136	162.5
operating mode	CW	CW
coupling parameter/β	0.76	—
unload Q_0	7400	—
$Q_{\rm L}$	4200	$\sim 5\times10^5$
bandwidth/Hz	39×10^3	$\sim$325
intermediate/MHz frequency	30.72	30.72
power of RF amplifier/dBm	46	—
power of pick up signal/dBm	10	10
frequency loop/Hz	—	$\sim$10

The amplitude and phase control loops are implemented using PI algorithm implemented in a Stratix-III FPGA. When the loops are settled and closed, the phase and amplitude can be locked for the set value. The results of the 12-hour test are shown in Fig. 7. The amplitude stability of the cavity field is less than $\pm0.32\%$, and the phase stability is ±0.35 degrees (peak to peak). The phase test result shows a monotonically decreasing trend over 12-hr. The main reasons for this is the decreasing environment temperature, and the temperature drift of reference signal provided by a power splitter outside the control test loop. In the future, the LLRF system will work with an SRF cavity in 4 K temperature. It will be much different from the parameters of Table 1. For example, as a result of increasing the loaded-Q, the cavity bandwidth will be substantially lower, so the loop parameters will be modified. The loop control may be more difficult, especially for the tuner, which will be a challenge between precision and response speed.

5 Summary

This LLRF control system is our first generation prototype based on digital I/Q technology. The twelve-hour test results demonstrate that an amplitude stability of $\pm0.32\%$ (peak to peak), $\pm0.18\%$ (RMS), and a phase stability of $\pm0.35^\circ$ (peak to peak), $\pm0.09^\circ$ (rms) could be achieved. The performance of this LLRF test system meets the expectations for this set of warm cavity measurements. In our future plans, we shall develop an RF front-end based on discrete components and integrated circuits, improve the reliability of LLRF, acquire and debug the loop PI parameters in a 4 K environment and optimize the algorithms.

References

1 Adam Molzahn Digital Phase Detection in a Variable Frequency RF System. Master Thesis. Department of Electrical and Computer Engineering of Michigan State University December 2005
2 Ken Kundert. Predicting the Phase Noise and Jitter of PLL-Based Frequency Synthesizers. Designer's Guide Consulting, Inc
3 Gardner F M, Phaselock Techniques, Second Edition. John Wiley & Sons, 1979, 112–113
4 MA J, LI M, Marlett M. A New Measurement and Analysis Method for a Third-Order Phase Looked Loop Transfer Function. IEEE International Test Conference, 2005
5 http://www.altera.com.cn/products/devkits/altera/kit-st3-dsp.html
6 http://www.thinksrs.com/