Active inductor shunt peaking in high-speed VCSEL driver design [*]

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Abstract: An all-transistor active-inductor shunt-peaking structure has been used in a prototype of 8 Gbps high-speed VCSEL driver which is designed for the optical link in ATLAS liquid Argon calorimeter upgrade. The VCSEL driver is fabricated in a commercial 0.25 μm Silicon-on-Sapphire (SoS) CMOS process for radiation tolerant purpose. The all-transistor active-inductor shunt-peaking is used to overcome the bandwidth limitation from the CMOS process. The peaking structure has the same peaking effect as the passive one, but takes a small area, does not need linear resistors and can overcome the process variation by adjust the peaking strength via an external control. The design has been taped out, and the prototype has been proven by the preliminary electrical test results and bit error ratio test results. The driver achieves 8 Gbps data rate as simulated with the peaking. We present the all-transistor active-inductor shunt-peaking structure, simulation and test results in this paper.

Key words: active inductor, shunt peaking, high-speed VCSEL driver, ASIC

1   Introduction

In the High Energy Physics (HEP) experiments, such as the ATLAS, all on-detector electronics systems and devices require the radiation tolerant characteristic. However, the radiation tolerant characteristic is usually beyond the concern of commercial products. To meet the requirements, some radiation tolerant commercial products have been proven and some radiation tolerant ASIC (Application Specific Integrated Circuit) chips have been designed.

A VCSEL (Vertical-Cavity Surface-Emitting Laser), which converts electrical signals into optical, is a key component in HEP optical communication links. Its driver amplifies the input signal to meet the requirements of a VCSEL. Nowadays, the commercial VCSEL drivers have a 10 Gbps transmission data rate or higher. However, in the HEP applications, the current fastest radiation tolerant VCSEL driver is GBLD [1], which is designed to work up to 5 Gbps with a 130 nm CMOS technology.

We designed a prototype of a radiation tolerant high-speed VCSEL driver to work at 8 Gbps data rate for the optical link in ATLAS liquid Argon calorimeter upgrade. A commercial 0.25 μm Silicon-on-Sapphire (SoS)

CMOS process has been used in the design for its radiation tolerant characteristic. The SoS process does not have a transient frequency (f_T) as fast as the newest process which is commonly used in commercial VCSEL drivers. The bandwidth extension methods must be used to achieve the transmission data rate. Our prototype design proves that the all-transistor active-inductor shunt-peaking structure can help the driver to achieve the target data rate and overcome the process variations. The technique detail is discussed in Section 2. Simulation results are shown in Section 3, and on chip preliminary electrical test results are shown in Section 4. A summary is in Section 5.

2   Design of active shunt peaking

The VCSEL driver in our design needs to receive low swing Current-Mode Logic (CML) signals (minimum 2 mA) from the line driver in the optical link and drive high swing CML signals (up to 8 mA) to the VCSEL at 8 Gbps. The targets are required by the optical link. The active inductor shunt peaking is the main method to achieve the data rate with the process we use. For other design details, please refer to our related work [2].
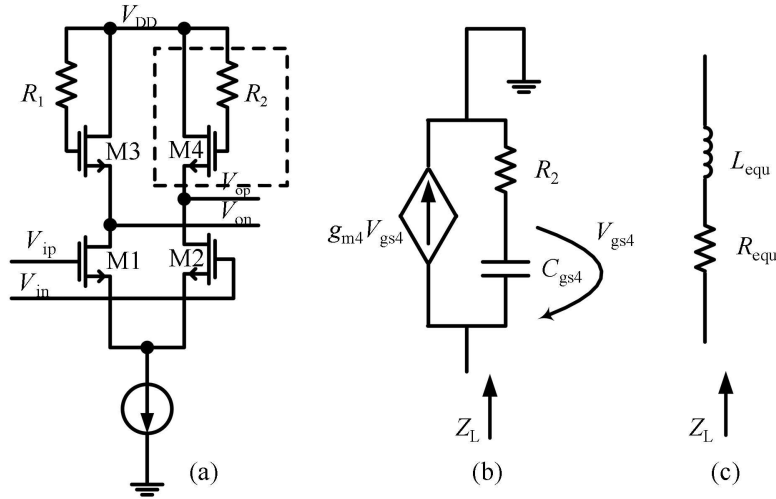
Fig. 1.   Conventional active shunt peaking: (a) topology; (b)high frequency small signal model; (c) passive equivalent circuit.

The shunt-peaking techniques are widely used to extend the bandwidth. A passive shunt-peaking technique can increase the circuit's bandwidth by nearly 80% with an inductor in series with a resistor load [3]. Even though the on chip inductor is available in our process, it is really inconvenient to use the on chip inductor due to its very large area. Usually, an active inductor, where a transistor combined with a resistor in Fig. 1(a), can be used to overcome the inconvenience of size and accomplish the shunt-peaking effect [4].

Figure 1(b) is the high frequency small signal model of the conventional active shunt-peaking topology in Fig. 1(a). When calculating the equivalent impedance, we apply a test voltage V_x at the bottom of the model where is the source of the nMOS M4 in Fig. 1(a), and easily get Eq. (1) and (2). During the calculation, we can cancel the V_{gs4}, which voltage crosses the C_{gs4}, and get the equivalent impedance Z_L as shown in Eq. (3).

$$\frac{V_{gs4}}{V_x} = \frac{\dfrac{1}{j\omega C_{gs4}}}{R_2 + \dfrac{1}{j\omega C_{gs4}}}, \qquad (1)$$

$$I_x = g_{m4}V_{gs4}, \qquad (2)$$

$$Z_L = \frac{V_x}{I_x} = \frac{1}{g_{m4}} + \frac{j\omega C_{gs4}R_2}{g_{m4}}. \qquad (3)$$

The first term in Eq. (3) is a resistor (R_{equ}), and the second term is an inductor (L_{equ}). The passive equivalent circuit of the conventional active shunt-peaking topology is the same as in the passive-inductor shunt-peaking technique, shown in Fig. 1(c).

The equivalent circuit and the capacitive load form a 2nd order RLC network which has a pole in the frequency response. The pole moves the cut-off frequency

to a higher range than no peaking case.

From Eq. (3), we know the equivalent inductor is determined by g_{m4}, C_{gs4} and R_2. The process variation of a resistor is larger than the other two factors, especially in our SoS process.

To overcome the variation drawback, we use a triode-biased pMOS to replace the resistor shown in Fig. 2. The gates of pMOS M5, M6 have been connected together to an external control pin (V_{ctrl}). By adjusting the voltage applied on the gate, we control the equivalent resistance in order to tune the peaking strength.
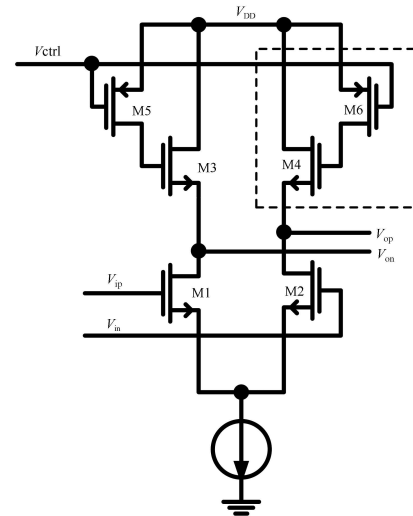

Fig. 2. All-transistor active-inductor shunt-peaking topology.

From the analysis above, we have an all-transistor active-inductor shunt-peaking structure which has the benefit of the passive inductor and only takes a small area. The peaking strength is tunable because of the use

of a controllable pMOS instead of a resistor. The tunable peaking strength makes it possible to overcome all the process variations and temperature changes.

3   Post-layout simulations

We optimized the peaking structure by scanning the parameters of MOSFETs in simulations inside of mathematics. Then we did the post-layout transient simulation of the full VCSEL driver design. In the simulation test bench, the input signal is an 8 Gbps PRBS-7 pattern with 2 mA differential current swing. All the effects from the parameters of the wire-bonding inductor, package capacitor and so on have been taken into consideration.

Shown in Fig. 3 is a current eye diagram at the VCSEL load at 27 ℃ typical process corner with default peaking strength from the post-layout simulation. The deterministic jitter (D_j) is 4.124 ps, and the eye vertical opening is 7.751 mA (775.1 mV on 100 Ω load). The output is fine to drive a physical VCSEL.
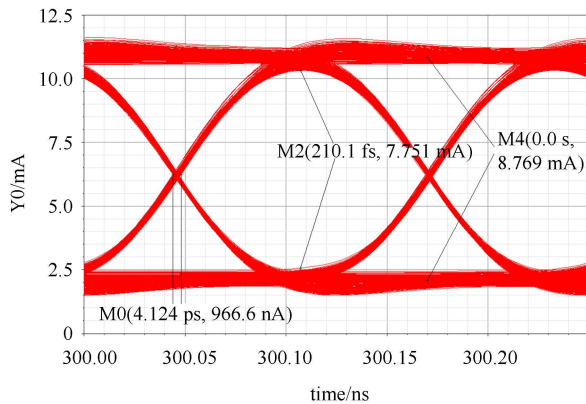
Fig. 3.   An eye diagram of current passing the VCSEL load at 27 ℃ typical process corner.

The peaking strength can be adjusted by the V_{ctrl} pin, and a series of simulations have been preformed to ensure the tunable peaking strength could cover all the process variations and temperature changes. We run simulation scripts to scan all nine pre-defined process corners and three typical temperatures (27 ℃, 55 ℃, 85 ℃).

Because of the type of MOSFET we use in the peaking structure, the pre-defined process corner — slowNfastPslowO is the worst one in all simulations. High temperature also affects the circuit functions most. We use the simulation results of 85 ℃ slowNfastPslowO process corner to demo the coverage of the tunable peaking strength. The tendencies of the deterministic jitter (D_j) and the vertical eye opening of the output current signal at different peaking control voltages (V_{ctrl}) are shown in Fig. 4.

In all the process corners and temperatures, not only the 85 ℃ slowNfastPslowO process corner, the simulation results have the similar tendencies. In each tendency

curve, we can find a best V_{ctrl} to balance the jitter and eye opening. The active shunt-peaking function works as we expected.
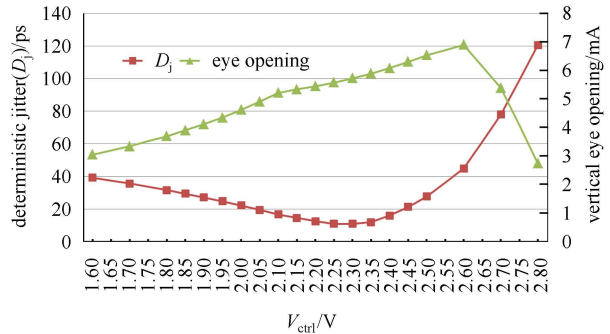
Fig. 4.   (color online) Peaking control tendencies in 85 ℃ slowNfastPslowO process corner.

4   On chip tests and results

Some quick tests have been done when the chip was fabricated in a Multi Project Wafer (MPW) run.

The test bench of an electrical test is shown in Fig. 5. The input signal is a 200 mV differential 8 Gbps PRBS-7 pattern which is provided by a pattern generator and attenuators. The input is AC coupled to the test PCB and the output is AC coupled to a sampling oscilloscope. The VCSEL driver has all the default settings except the peaking control.
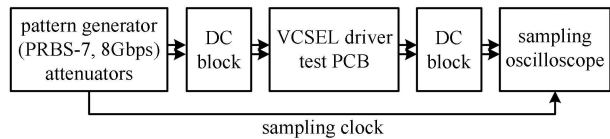
Fig. 5.   Test bench of an electrical test.

The eye diagram of the electrical output and jitter analysis from the sampling oscilloscope are shown in Fig. 6. When the chip was taped out, we didn't know the exact process variation for each chip, and we cannot compare the test results with any existing simulation results directly.

The total jitter of the eye diagram is about 24.469 ps and the eye vertical opening is about 600 mV on 100 Ω load. These test results are close to our simulation results.

Different external peaking control voltages are used in the test, and the tendency is close to the simulation.

We finished a bit error ratio test (BERT) with our driver driving a commercial 10 Gbps VCSEL. The optical fiber and receiver used in the test are all commercial
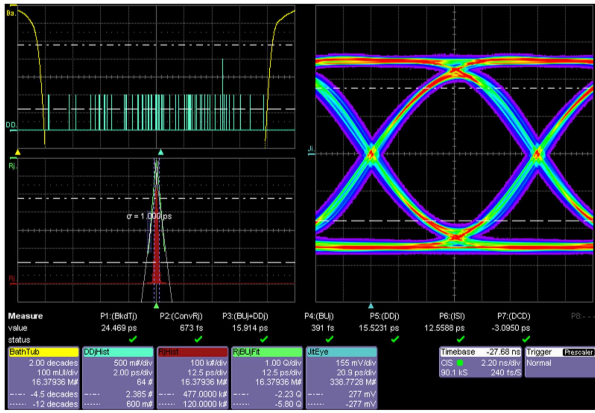
Fig. 6.   (color online) Eye diagram and jitter analysis in an electrical test.

products which have a data rate higher than 8 Gbps. So if an error occurs during the test, it may be mainly caused by the driver. The test results are shown in Table 1.

The target data rate of our design is 8 Gbps, and a bit error ratio is required to be smaller than 10^{-12} from the industrial standard. From the test results, the driver can work at 10 Gbps with a bit error ratio smaller than the industrial standard in a long time test.

As a prototype, the design is successful from the above test results. The next version with digital configuration has been prepared based on this prototype.

Table 1.   Results of optical bit error ratio tests.

data rate/ Gbps	test time/s	total bits	errors	error ratio
5.0	300	1.50×10^{12}	0	$<6.67 \times 10^{-13}$
8.0	300	2.40×10^{12}	0	$<4.17 \times 10^{-13}$
10.0	300	3.00×10^{12}	0	$<3.33 \times 10^{-13}$
10.0	54000	5.40×10^{14}	6	1.11×10^{-14}
10.5	300	3.15×10^{12}	3	9.52×10^{-13}

5   Conclusion

With the use of all-transistor active-inductor shunt-peaking structure, we successfully designed a prototype of an 8 Gbps VCSEL driver with a commercial 0.25 μm SoS CMOS process for radiation tolerant purpose in the optical link in ATLAS liquid Argon calorimeter upgrade. It is proven that the peaking structure can overcome the bandwidth limitation and process variations. The peaking function works as we expected from the preliminary electrical test results. The bit error ratio test passes the industrial standard. The prototype provides a good reference for the next version of our radiation tolerant VCSEL driver design.

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