Radiation induced inter-device leakage degradation

HU Zhi-Yuan(胡志远)[1,2;1)] LIU Zhang-Li(刘张李)[1,2] SHAO Hua(邵华)[1]
ZHANG Zheng-Xuan(张正选)[1] NING Bing-Xu(宁冰旭)[1,2] CHEN Ming(陈明)[1,2]
BI Da-Wei(毕大炜)[1] ZOU Shi-Chang(邹世昌)[1]

[1] Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China
[2] Graduate University of Chinese Academy of Sciences, Beijing 100049, China

Abstract: The evolution of inter-device leakage current with total ionizing dose in transistors in 180 nm generation technologies is studied with an N-type poly-gate field device (PFD) that uses the shallow trench isolation as an effective gate oxide. The overall radiation response of these structures is determined by the trapped charge in the oxide. The impacts of different bias conditions during irradiation on the inter-device leakage current are studied for the first time in this work, which demonstrates that the worst condition is the same as traditional NMOS transistors. Moreover, the two-dimensional technology computer-aided design simulation is used to understand the bias dependence.

Key words: total ionizing dose, shallow trench isolation, PFD device, 2-D simulation

PACS: 07.80.+b, 24.50.+g **DOI:** 10.1088/1674-1137/35/8/013

1 Introduction

Shallow trench isolation (STI) was introduced at the 0.25 μm technology node to reduce the spacing between adjacent devices compared with the older LOCOS isolation process. As it is scaled down, the gate oxide becomes thinner and less sensitive to the total ionizing dose (TID) irradiation. Numerous publications [1–3] have demonstrated that the reduction in gate oxide thickness essentially eliminates the radiation induced degradation related to the gate oxide. However, the STI does not scale down correspondingly. More sizable TID effects are instead associated with the lateral STI oxides, which are about two orders of magnitude thicker [4]. Therefore, the STI has become by far the most important part for the total dose radiation hardening in modern CMOS technologies.

Radiation induced STI oxide degradation results in two leakage paths: intra-transistor leakage and inter-device leakage, which are shown in Fig. 1. The former has been widely studied [5–8]. Radiation induced positive trapped charge in the isolation dielectric, particular at the Si/SiO_2 interface along the sidewalls of the STI trench, inverts the edge of the channel and creates a leakage path which becomes the dominant contributor to off-state drain-to-source leakage current in n-channel MOSFETs (NMOS). This leakage degrades transistor switching performance and eventually leads to functional transistor failures. The latter is not given much attention, which is studied only by a few publications [9].

The cited study worked on the comparison of these two leakages at high dose and figured out a

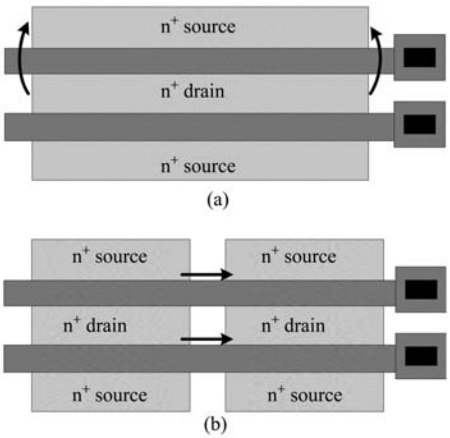

Fig. 1. Schematic illustration of intra-transistor leakage (a) and inter-device leakage (b).

Received 17 November 2010
1) E-mail: zhiyuan@gracesemi.com

good correlation between the TID response of sidewall and bottom of the STI (i.e., a channel is created underneath field oxides allowing current flow between transistors that normally are isolated).

This paper gives additional knowledge about the radiation induced inter-device leakage current, including the bias mode dependence and the bias stress magnitude dependence. Also two-dimensional device simulations are used to obtain insights into the electric field to illustrate the physical basis for bias conditions dependence.

2 Experimental details

2.1 Test structures

The test devices were specially developed for studying the inter-device leakage from a 180 nm CMOS technology. Fig. 2 illustrates the schematic cross-section of the test device, which is similar to the traditional NMOS transistor but using the thick STI oxide with a thin gate oxide as the gate dielectric instead. We call it the N-type poly-gate field device (PFD). This device is in fact a parasitic transistor in ICs and is very important for monitoring the leakage current related to the STI isolation. That means worse STI isolation will induce a bigger leakage current which increases the power consumption and even causes functional failures of the integrated chips.

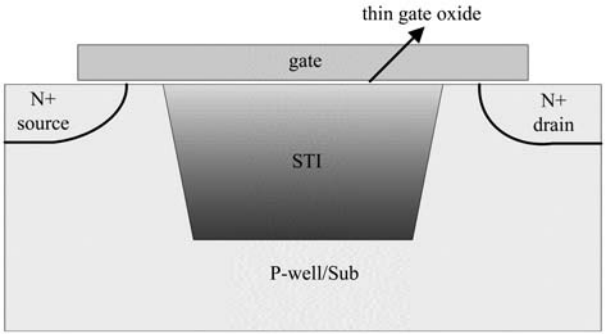

Fig. 2. Cross-section of the N-type PFD, which uses the STI oxide with a thin gate oxide as its effective gate dielectric.

STI used for field isolation is filled by high density plasma oxide. The STI with very steep sidewalls ($\sim 87°$) has a thick oxide about 390 nm. The thin gate oxide under the gate of the PFD is less than 3 nm and the source and drain are highly N-type doped. The width and length of the PFD in our work are 50 μm and 0.28 μm, respectively. The operating voltage is 1.8 V. Furthermore, all the samples are ceramics packaged.

2.2 Irradiation and measurement setup

The experiments were conducted at the Xinjiang Technical Institute of Physics and Chemistry, the Chinese Academy of Sciences and ^{60}Co γ-ray was used as the radiation source. During the γ-ray irradiation, the PFD transistors were biased at different bias conditions, which are summarized in Table 1. The ON, OFF and PASS modes correspond to on-state, off-state of PFD device and transmission-gate like access transistors in memory cells, respectively. The ON_low mode is just the ON mode with a lower gate voltage. And the GROUND mode means that all the terminals are grounded. The dose rate was typically around 205 rad(Si)/s and the total dose levels achieved were 1 Mrad(Si).

Table 1. Bias condition definition for PFD device.

type	gate/V	source/V	drain/V	substrate/V
ON	1.8	0	0	0
OFF	0	0	1.8	0
PASS	0	1.8	1.8	0
ON_low	0.9	0	0	0
GROUND	0	0	0	0

Before irradiation and after every irradiation step, *I-V* characteristics of the devices were measured by HP4140B parameter analyzer at room temperature. The test condition was: gate and substrate are floating, $V_{\rm source}$=0 V, sweep $V_{\rm drain}$=0–5 V. The time between two irradiation steps was controlled within half an hour.

The Synopsys technology computer-aided design (TCAD) tools were used to provide a 2-D simulation of the device structure. The structure profile and dimension were determined by the design and process conditions. A retrograde well was used. The source and drain included extensions and halo implants. The source, gate, drain and substrate voltages were provided as boundary conditions.

3 Experimental results and discussions

3.1 $I_{\rm DS}$-$V_{\rm DS}$ characteristic

In Fig. 3, the $I_{\rm DS}$-$V_{\rm DS}$ curve of the PFD device as a function of TID for the ON bias mode is plotted. The $I_{\rm DS}$ means the current flowing from the drain to the source and the $V_{\rm DS}$ represents the potential difference between the drain and the source. As the total dose level increases, the leakage current increases. The physical processes from the initial deposition of

energy by ionizing radiation to the creation of ionization defects are: 1) the generation of e-h pairs; 2) the prompt recombination of a fraction of the generated e-h pairs; 3) the transport of free carriers remaining in the oxide; and 4) the formation of trapped charge via hole trapping in defect precursor sites and the formation of interface traps via reactions involving hydrogen. The positive oxide trapped charges will invert a channel along the STI, which forms a leakage path between the source and drain. As the total dose increases, more oxide trapped charges are built up in the oxide, which enhances the leakage current.

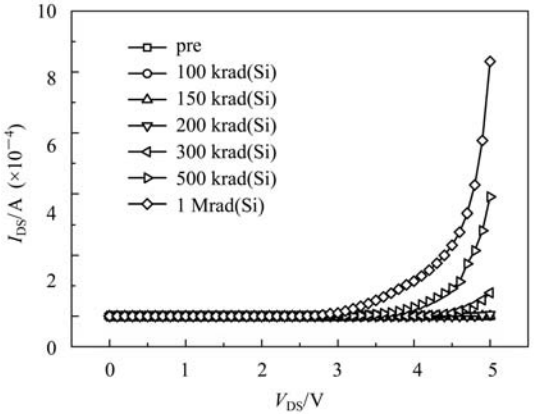

Fig. 3. I_{DS}-V_{DS} characteristic of PFD device as a function of TID. During the test, the gate and substrate are floating and the source is grounded.

The leakage current (when V_{DS}=5 V) is extracted as shown in Fig. 4. It increases 4 orders and reaches almost 800 μA at a dose level of 1 Mrad(Si), which is beyond the circuit tolerance. In fact, V_{DS}=5 V is a harsh condition; for the normal and actual operation, the V_{DS} is equal to 1.8 V. The inset in Fig. 4 is the leakage current at V_{DS}=1.8 V which shows that the leakage current is less than 0.1 nA even up to a dose level of 500 krad(Si). This result gives a good indication that inter-device leakage should not threaten the functionality of most ICs in moderate dose rate environments.

For the intra-leakage current, when the oxide trapped charge in the STI sidewalls inverts the edge of the channel, the leakage will increase significantly. While for the inter-leakage current, not only the STI sidewalls but also the STI bottom should trap enough oxide trapped charges to invert the channel, then a significant leakage current can be observed from the drain to source. As the STI bottom is far away from the gate, the electric field in this location is reduced. This makes the initial recombination play a very important role in this area; then the radiation induced oxide trapped charge is small. So it is harder to form a leakage path for the inter-leakage than for the intra-leakage.

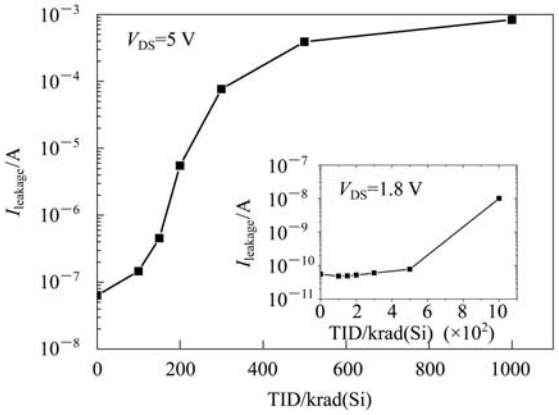

Fig. 4. PFD leakage current as a function of TID at a harsh condition (V_{DS}=5 V) and a normal operation condition (V_{DS}=1.8 V).

3.2 Bias mode dependence

The leakage current in different bias modes including the ON bias, OFF bias and PASS bias as a function of TID is compared in Fig. 5. The results clearly indicate that the ON bias mode is the worst case while OFF bias is comparable with PASS bias, which is the same as the traditional NMOS transistors [10]. All the samples in this work were fabricated in the same wafer, so it is reasonable to assume that they have the same STI profile. The only difference is the electric field during irradiation. In order to clarify this difference clearly, the electric field is simulated using the TCAD simulation as shown in Fig. 6. First, the electric field directions have some difference. For the ON bias mode, the electric fields lines originate from the STI terminate to the source and drain along the sidewalls (except the STI corner). While for the OFF and PASS bias, some electric field lines in the middle of the sidewalls point to the opposite direction, that are originating from the source and drain terminates to the STI. For the ON bias mode, the positive charges are pushed to the STI interface along the whole sidewalls (also not considering the STI corner). While in the middle of the STI sidewalls for the OFF and PASS bias modes, some of the charges are likely to be pushed to the opposite direction. The oxide trapped charge away from the interface is less effective in altering the electrical characteristics of the channel. Secondly, the electric field magnitude is different. Take the electric field along the STI sidewalls (the arrow as shown in Fig. 6(a)) as an example. The electric field magnitude of the three bias modes is

compared in Fig. 6(b). The results show that the ON bias mode has the most intense electric field, which strongly influences the initial recombination. In other words, the applied field determines the charge yield immediately after e-h pairs are created by the radiation interacting with the trench oxide. As the charge yield is proportional to the applied field [11], a lower electric field results in a lower charge yield, then less oxide trapped charge is trapped along the trench sidewalls.

The bias modes experiments on PFD devices show it is similar to the traditional transistors (both show a leakage increase and to be worst in the ON bias mode). So the PFD devices can be effectively used to study the properties of the trapping centers responsible for the NMOS intra-transistor leakage current.

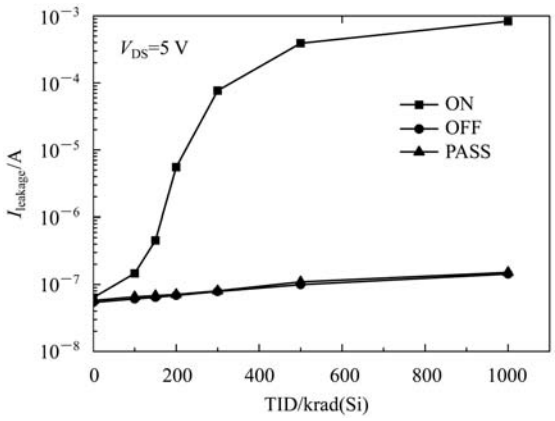

Fig. 5. The leakage current of PFD as a function of TID for ON bias, OFF bias and PASS bias modes.

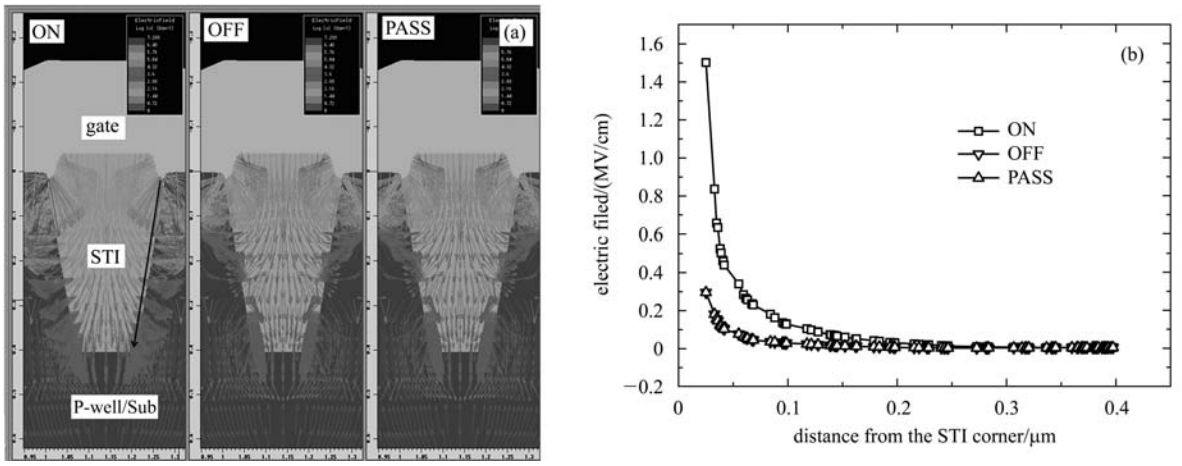

Fig. 6. (a) TCAD simulation of electric filed lines distribution for the ON bias, OFF bias and PASS bias modes. (b) The electric filed magnitude along the arrow in (a) for the three bias modes.

3.3 Bias stress magnitude dependence

Results on the PFD devices presented in Fig. 5 have been obtained with the gate biased at supply voltage V_{dd} (1.8 V) and with all the other terminals grounded. Nominally identical devices have also been irradiated with the gate at 0.9 V and 0 V (that is ON_low and GROUND bias modes in Table 1), to study the influence of the transistor bias stress condition on the TID response. The results are shown in Fig. 7, where the leakage current of the PFD device is shown as a function of the TID for the three bias conditions.

At 0.9 V the degradation is less pronounced for the PFD device. The electric filed in the STI has still an important influence on the PFD device whose inter-leakage current is almost 10% of the worst case.

When the gate is grounded during irradiation, we can see that the degradation is strongly reduced. The leakage current is around 0.2 μA for TID up to 1 Mrad(Si) for a harsh test condition (V_{DS}=5 V).

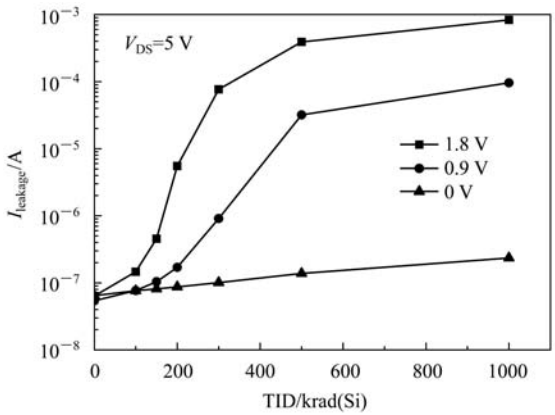

Fig. 7. The gate bias stress impact on the leakage current of the PFD device.

The reason for this dependence on the bias stress is that smaller potentials applied to the gate lead a

decrease of the electric field across the STI of the PFD device, which is shown in Fig. 8. The maximum electric field of the ON_low bias is about 50% smaller than the ON bias and the GROUND bias is only 20% of the worst case. The reduction allows the recombination of a greater number of e-h pairs generated by the ionizing radiation in the oxide, leaving less charge available for trapping in the defect centers.

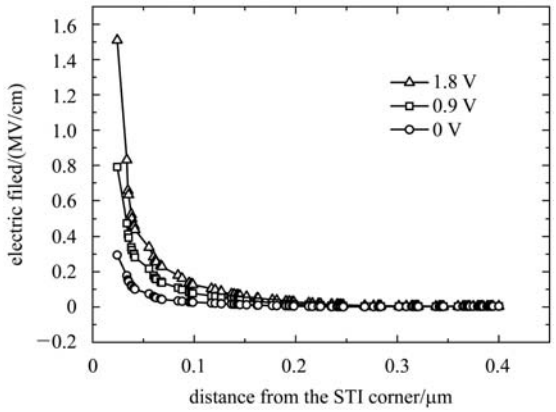

Fig. 8. TCAD simulation of the electric field along the STI sidewalls for the three bias stress conditions.

These results also show the same trend with the traditional NMOS transistors, which again confirms that the inter-device leakage of the PFD device provides a good correlation with the intra-transistor leakage.

The PFD devices could also be used as a radiation detector. As shown in Fig. 4, the leakage current increases monotonously with the TID dose level. In other words, there is a one-to-one correspondence between the leakage current and the TID dose level. Consequently, we should first calibrate the relationship between the leakage of the PFD devices and the TID dose level by using a standard radiation source, then the total dose level could be deduced by measuring the leakage current of the PFD devices in a arbitrary radiation environment. It should be noted that the device should be annealed at high temperature to remove the charge trapped in the oxides [9] before the next detection. In order to achieve high accuracy, the leakage current should be sensitive to the total dose. So the ON bias mode ($V_{\rm gate}$=1.8 V, $V_{\rm drain}$ = $V_{\rm source}$ = $V_{\rm substrate}$=0 V) during irradiation and the harsh condition ($V_{\rm DS}$=5 V with other terminals floating) during the test is the best choice. While at non-working status, all the terminals should be floating to ensure that no possible charge can be trapped in the oxide.

4 Conclusions

We have studied the inter-device leakage current on the N-type poly-gate field devices in a 180 nm CMOS technology. The leakage increases with increasing the total ionizing dose because the oxide trapped charge is trapped at the trench sidewalls. The bias conditions dependence including the ON, OFF and PASS bias modes and the bias stress magnitude on the leakage is studied. TCAD simulation is used to help us to analyze the experiment results. The bias modes experiments on PFD devices show it is quite similar to the traditional NMOS transistors, which suggest that studying the inter-device leakage current is a good reference to the properties of the trapping centers responsible for NMOS source-drain leakage. For radiation detector application, the PFD devices should be irradiated in ON bias mode and tested at harsh conditions to obtain a higher accuracy.

References

1 Brady F T, Maimon J, Hurt M. IEEE Trans. Nucl. Sci., 1999, **46**: 1836
2 Manghisoni M, Ratti L, Re V, Speziali V, Traversi G, Candelori A. IEEE Trans. Nucl. Sci., 2003, **6**: 1827
3 Re V, Manghisoni M, Ratti L, Speziali V, Traversi G. IEEE Trans. Nucl. Sci., 2006, **53**: 1599
4 Faccio F, Cervelli G. IEEE Trans. Nucl. Sci., 2005, **52**: 2413
5 Shaneyfelt M R, Dodd P E, Draper B L, Flores R S. IEEE Trans. Nucl. Sci., 1998, **45**: 2583
6 McLain M, Barnaby H J, Holbert K E, Schrimpf R D, Shah H, Amort A, Baze M, Wert J. IEEE Trans. Nucl. Sci., 2007, **54**: 2210
7 EN Y F, LIN C L, LUO H W, QIAN C, SHI Q, WANG X, WANG X H, WANG Y M, ZHANG E X, ZHANG Z X, ZHAO G R. Chin. Phys., 2006, **15**: 792
8 LI D M, WANG Z H, Huangfu L Y, GUO Q J. Chin. Phys., 2007, **16**: 3760
9 Faccio F, Barnaby H J, CHEN X J, Fleetwood D M, Gonella L, Mclain M, Schrimpf R D. Microelectronics Reliability, 2008, **48**: 1000
10 Witczak S C, Lacoe R C, Osborn J V, Hutson J M, Moss S C. IEEE Trans. Nucl. Sci., 2005, **52**: 2602
11 Boesch H E, McGarrity J M. IEEE Trans. Nucl. Sci., 1976, **23**: 1520