Radiation response of pseudo-MOS transistors fabricated in hardened fully-depleted SIMOX SOI wafers*

BI Da-Wei(毕大炜)[1)] ZHANG Zheng-Xuan(张正选) ZHANG Shuai(张帅) CHEN Ming(陈明)
YU Wen-Jie(余文杰) WANG Ru(王茹) TIAN Hao(田浩) LIU Zhang-Li(刘张李)

(The State Key Laboratory of Functional Materials for Informatics,
Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China)

Abstract The total dose radiation response of pseudo-MOS transistors fabricated in hardened and unhardened FD (fully-depleted) SIMOX (Separation by Implanted Oxygen) SOI (Silicon-on-insulator) wafers is presented. At 1 Mrad(Si) radiation dose, the threshold voltage shift of the pseudo-MOS transistor is reduced from -115.5 to -1.9 V by the hardening procedure. The centroid location of the net positive charge trapped in BOX, the hole-trap density and the hole capture fraction of BOX are also shown. The results suggest that hardened FD SIMOX SOI wafers can perform well in a radiation environment.

Key words SOI, pseudo-MOS transistor, total dose radiation, ion implantation

PACS 07.89.+b, 81.07.Bc

1 Introduction

Silicon-on-insulator (SOI) technology has many great advantages over bulk-silicon technology for radiation-hardened military and space applications. Transistors and circuits made of SOI materials are resistant to single-event and dose rate effects in a high leve1[1]. Unfortunately, the existence of buried oxide (BOX) introduces a total dose problem. The radiation-induced positive charge trapped in the BOX leads to the back channel conduction of a fully-depleted (FD) SOI transistor, which increases the leakage current and induces the threshold voltage shift[2].

Ion implantation of BOX with silicon is an effective method to enhance the resistant ability of SOI materials to the total dose radiation. Ion implantation creates electron traps with large capture cross sections, that, when filled, could compensate the radiation-induced trapped positive charge in the BOX[3]. The pseudo-MOS transistor is essentially a test device for the characterization of SOI wafers. Highly pure transistor-like characteristics can be obtained from which the electrical parameters of the film, BOX and top interface can also be extracted[4—7].

In this work, pseudo-MOS transistors and SIS (semiconductor-insulator-semiconductor) capacitors were fabricated in ultra thin FD SIMOX (Separation by Implanted Oxygen) SOI wafers hardened or unhardened by silicon ion implantation. The total dose response of the devices mentioned above was investigated under ^{60}Co γ ray radiation, which aimed to evaluate the radiation hardness of the ultra thin SOI wafers. We also discussed the effects of the hardening procedure on the charge centroid location and the hole-trap density of BOX.

2 Experiment details

The Si film and BOX thicknesses of FD SIMOX SOI wafers used in this experiment are 50 nm and 380 nm respectively. The wafers were hardened by implanting Si ions at a dose of $1\times10^{15}/\mathrm{cm}^2$ into BOX followed by a 950 ℃ anneal.

Received 22 December 2008

* Supported by Major State Basic Research Development Program

1) E-mail: davidb@mail.sim.ac.cn

The pseudo-MOS transistors were fabricated as shown in Fig. 1. The isolated silicon islands were formed by the definition, etching, and cleaning of the top Si film. The principle of the pseudo-MOS transistor is very simple: the bulk Si substrate is biased as a gate contact through a metal support, the BOX acts as the gate oxide and the Si film is the transistor's body serving simultaneously as drain and source probe-contacts. Biasing the substrate induces an inversion or an accumulation conduction channel at the upper interface of the BOX, so that MOSFET-type electrical characteristics such as I-V curves are obtained. The SIS capacitors use the same fabrication mask as the pseudo-MOS transistors, except that aluminum is deposited on the top of the Si film. The transistors and capacitors yield the voltage shift information of both Si-BOX interfaces respectively during radiation, by which we can calculate the charge centroid location[8].

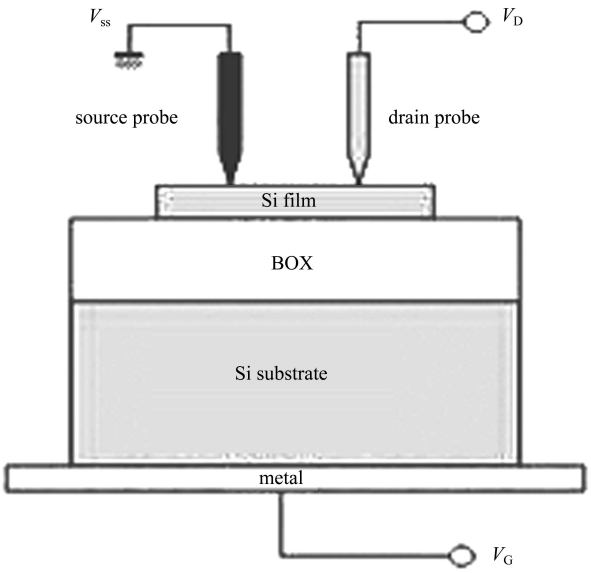

Fig. 1. Schematic diagram of a pseudo-MOS transistor with point probes for source and drain contacts.

Our samples were exposed to a ^{60}Co γ ray source at a dose rate of 25 krad(Si)/min for the total dose radiation testing. We applied a positive voltage on the metal (see Fig. 1) to create a strong biased electric field of 5×10^5 V/cm through BOX during radiation for trapping more holes. We used HP 4156C and 4284A parametric analyzers for measuring the I-V characteristics of transistors and C-V characteristics of capacitors respectively before and after radiation. The samples were characterized as a function of total dose at 0, 300, 600 and 1000 krad(Si).

3 Results and discussion

Figure 2 shows the I-V characteristic curves of unhardened and hardened pseudo-MOS transistors after suffering different radiation doses. The pseudo-MOS transistor exhibits behaviors similar to a combination of conventional pMOS and nMOS transistors. But in this paper, we focus on the voltage shift and leakage current information of the samples during radiation to evaluate the hardening technology. The other details of the curves are not major concerns in this research.

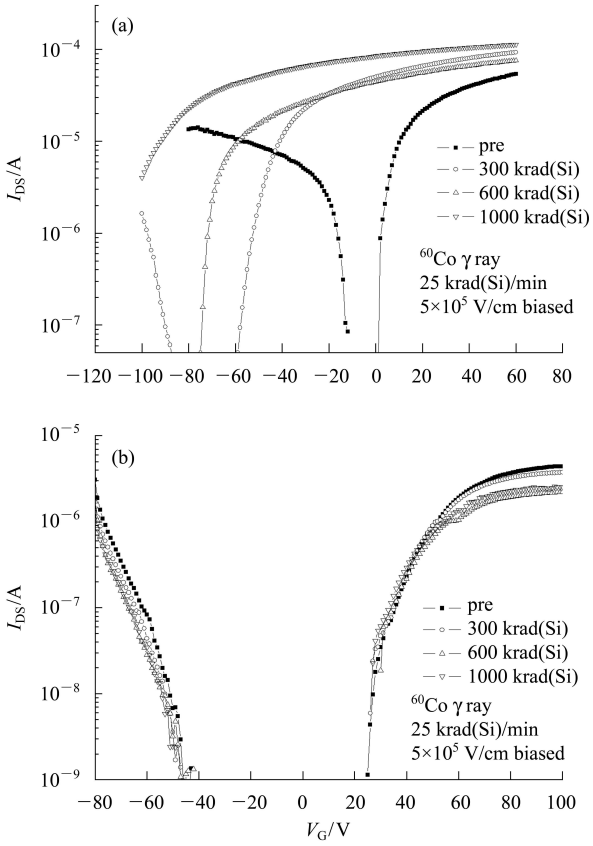

Fig. 2. I-V characteristic curves for (a) unhardened and (b) hardened pseudo-MOS transistors after different radiation doses at V_D= 0.1 V.

The curves of the unhardened pseudo transistor had a large negative shift during radiation, and the back channel current of the nMOS-like part at V_G=0 was saturated after only 300 krad(Si) radiation. This resulted in unbearable degradation of the top gate threshold voltage and large leakage current of front channel in conventional FD nMOS transistors fabricated in this material[9].

Little or no shift of curves was observed in the hardened pseudo transistor suffering radiation. No obvious current occurred even when V_G=20 V, elimi-

nating the coupling effect caused by the large radiation induced oxide charge in BOX. The differences of saturated current value were mainly due to the small change of probe pressure in each measurement[4].

Figure 3 shows the radiation response of capacitors. The negative shifts of curves are similar, indicating that the hardening procedure has a smaller effect on the bottom interface of BOX.

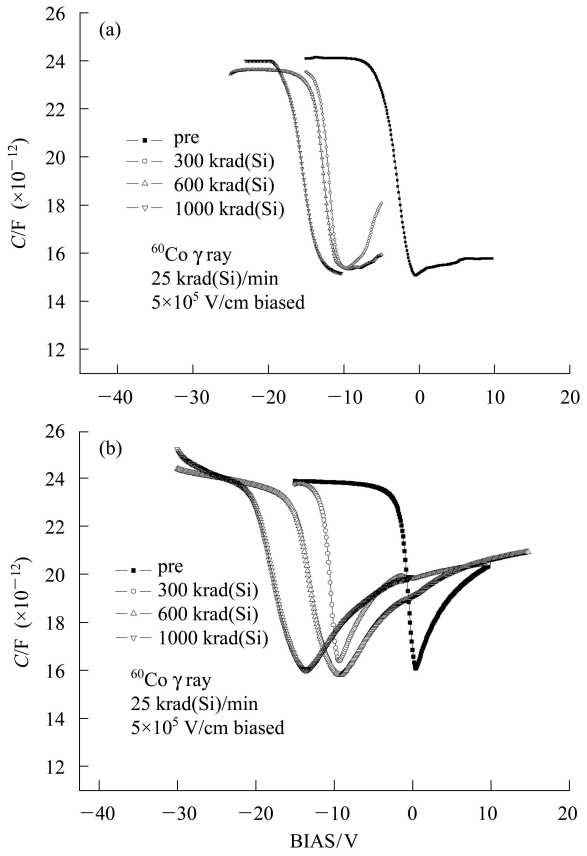

Fig. 3. *C-V* characteristic curves for (a) unhardened and (b) hardened capacitors after different radiation doses.

The threshold voltage shifts of pseudo transistors and flatband voltage shifts of capacitors as a function of total dose are given in Fig. 4. The maximum shift of the hardened transistor is shown to be −1.9 V at the dose of 1000 krad(Si). Compared with the −115.5 V shift of the unhardened transistor, it appears that the hardening procedure is very effective. We also see that the flatband voltage shifts are at the same level for both kinds of capacitors.

The net positive charge centroid locations of hardened and unhardened BOX after radiation were extracted with the data in Fig. 4, using the following equation[10]:

$$x = T_{\rm box}(1+\Delta V_{\rm th}/\Delta V_{\rm ft})^{-1}, \quad (1)$$

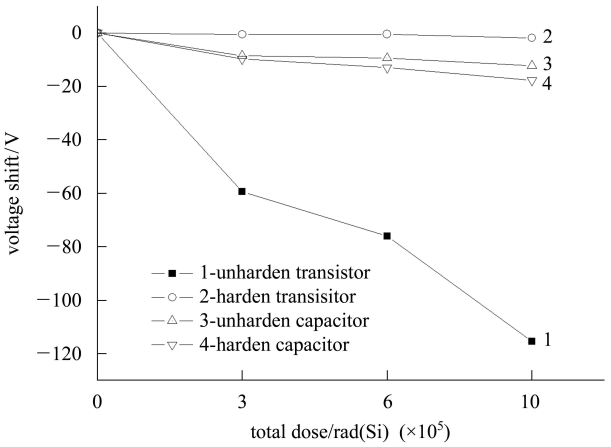

Fig. 4. Radiation induced voltage shift as a function of the total dose. (1) Threshold voltage shift of unhardened transistor. (2)Threshold voltage shift of hardened transistor. (3) Flatband voltage shift of unhardened capacitor. (4) Flatband voltage shift of hardened capacitor.

where $T_{\rm box}$ = 380 nm is the BOX thickness, $\Delta V_{\rm th}$ is the threshold voltage shift of the transistor and $\Delta V_{\rm ft}$ is the flatband voltage shift of the corresponding capacitor made in the same wafer after different radiation doses. The results are shown in Fig. 5.

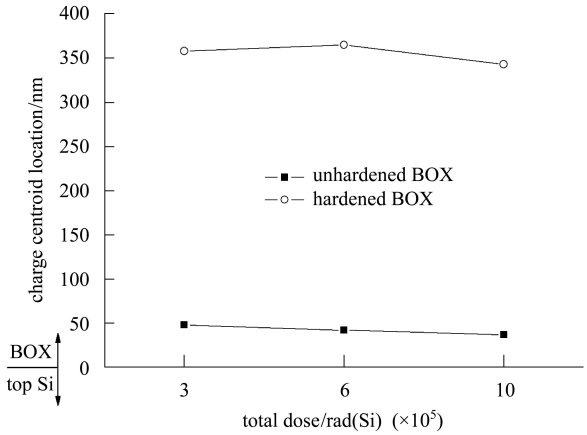

Fig. 5. The charge centroid location of hardened and unhardened BOX as a function of radiation dose.

We can see that the centroid locations of unhardened BOX are 48 nm, 42 nm and 37 nm beneath the top interface with increasing dose. The change of centroid location is due to the fact that the radiation induced holes drift toward the top interface under the applied strong electric field during radiation. It is so close to the back channel of the transistor that a large amount of trapped net positive charge can impact on the threshold voltage and leakage current badly, which is consistent with our results in Fig. 2(a).

In contrast, the centroid location of hardened BOX is about 350 nm, close to the bottom interface.

This is because a lot of filled electron traps created by the hardening procedure compensate the positive charge in the upper part of BOX. So the residual net positive charges in BOX have little effect on the threshold voltage as shown in Fig. 2(b).

Usually the $\Delta V_{\rm th}$ of a pseudo-MOS transistor can be described by the following equations[11]:

$$\Delta V_{\rm th}(D) = -A\left[1-\exp\left(-\frac{D}{D_0}\right)\right], \quad (2)$$

$$A = \frac{qN_{\rm ot}T_{\rm BOX}}{k\varepsilon_0}, \quad (3)$$

$$D_0 = \frac{\omega N_{\rm ot}}{\alpha T_{\rm BOX}\rho}, \quad (4)$$

where D is the total dose in rad(Si), and the parameter A is the maximum threshold voltage shift, usually occurring near 1000 krad(Si), and D_0 is another parameter, k is the oxide dielectric constant, ρ is the oxide density, and ω is the energy required to create an electron-hole pair. We fit Eq. (2) with the experimental data presented in Fig. 4 (curve1) and 4 (curve2), and then A and D_0 can be obtained.

In terms of Eqs. (3) and (4), parameter A is related to the hole-trap density $N_{\rm ot}$ and D_0 is related to the fraction of hole capture, α, a number which indicates the hardness of the BOX. We show the variations of the two radiation parameters, $N_{\rm ot}$ and α, in Table 1.

Table 1. Radiation parameters of SIMOX SOI pseudo-MOS transistors.

parameters	unhardened	hardened
A/V	147.86	3.07
D_0/rad^{-1}	7.23×10^5	3.27×10^5
$N_{\rm ot}$/cm^{-2}	8.52×10^{12}	1.77×10^{11}
α	0.042	0.0019

For the hardened transistor, at least a factor of 40 improvement in the hole-trap density and a factor of 20 improvement in the fraction of hole capture over the unhardened transistor are demonstrated. This fully explains that the hardening procedure is very effective in enhancing the resistant ability of FD SIMOX SOI materials to the total dose radiation.

4 Conclusions

In this paper, we analyzed the radiation response the pseudo-MOS transistors fabricated in hardened and unhardened FD SIMOX SOI wafers. We also calculated the centroid location of net positive charge trapped in BOX, the hole-trap density and the hole capture fraction of hardened and unhardened BOX. The results show that the hardening procedure is a very effective method to reduce the amount of net positive charge trapped in the BOX and enhance the hardness of the BOX of FD SIMOX SOI materials.

References

1 Auberton-Herve A J. SOI: Materials to Systems. In: IEEE IEDM technical digest. CA: USA, 1996. 3—10
2 Jenkins W C, LIU S T. IEEE Trans. Nucl. Sci., 1994, **41**(6): 2317
3 Mrstik B J, Gouker P, Lawrence R K et al. IEEE Trans. Nucl. Sci., 2003, **50**(6): 1947
4 Cristoloveanu S, Munteanu D, LIU S T. IEEE Trans. Nucl. Sci., 2000, **47**(5): 1018
5 Hefyene N, Cristoloveanu S, Ghibaudo G et al. Solid-State Electronics, 2000, **44**: 1711
6 JUN B, Fleetwood D M, Schrimpf R D et al. IEEE Trans. Nucl. Sci., 2003, **50**(6): 1891
7 Sato S, Komiya K, Bresson N et al. IEEE Trans. Nucl. Sci., 2005, **52**(8): 1807
8 Muller R S, Kamins T I. Device Electronics for Intergated Circuits. New Jersey: John Wiley Publishing Company, 1986. 400
9 Schwank J R, Ferlet-Cavrois V, Shaneyfelt M R et al. IEEE Trans. Nucl. Sci., 2003, **50**(3): 522
10 Lawrence R K, Ioannou D E, Hughes H L et al. IEEE Trans. Nucl. Sci., 1995, **42**(6): 2114
11 LIU S T, Jenkins W C, Hughes H L. IEEE Trans. Nucl. Sci., 1998, **45**(6): 2442