# A non-IQ sampling controller in low level RF system*

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**Abstract** This paper describes a non-IQ controller for digital Low Level RF (LLRF) feedback control. Based on this non-IQ sampling method, arbitrary frequency relationship between ADC/DAC sampling clocks and IF signals can be employed. The nonlinearity in digital conversion can be reduced and the system dynamic performance improved. This paper analyzes the nonlinearity in conventional IQ sampling, gives the state variable description of the non-IQ algorithm, presents an implementation and its synchronization, and compares its performances with IQ sampling.

**Key words** Shanghai synchrotron radiation facility, LLRF, non-IQ, field programmable gate array

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## 1 Introduction

LLRF has been playing an important role in RF systems of modern accelerators to maintain the proper cavity RF field conditions for acceleration. Instead of processing cavity amplitude and phase directly[1—3], In-phase and Quadrature (IQ) demodulation technique is usually used[4] Digital IQ demodulator implementation has advantages over analog demodulator implementation and is adopted recently[5].

In digital IQ demodulator implementation, the RF input is downconverted to an IF signal by mixing the RF with a Local Oscillator (LO) signal. The resulting signal is bandpass filtered to remove the high-frequency component that results from mixing and also limit the signal bandwidth to avoid aliasing. The output is sampled with an Analog-to-Digital Converter (ADC) operating at a particular frequency which corresponds to the phase shift between consecutive ADC samples of $(2n-1)\cdot 90^\circ$, $n=1,2,\cdots$. If we define the first sample as $I$, the ADC output provides a data stream consisting of the repeating pattern of measurements of $I$, $Q$, $-I$, $-Q$ or $I$, $-Q$, $-I$, $Q$. This digital IQ demodulation technique has been adapted to many LLRF systems. For example, LBNL has built the digital LLRF system for the spallation neutron source and obtained cavity amplitudes better than 1% and relative phases within $1^\circ$[6, 7]. As a third generation light source the Shanghai Synchrotron Radiation Facility (SSRF) has built a prototype of the digital LLRF system which maintains the cavity fields within $\pm 1\%$ amplitude error and $\pm 1^\circ$ phase error[8] under the cooperation with LBNL.

The accuracy of measurements of IQ signals in analog to digital conversion directly affects the operational stability and control of the RF system. One fundamental limitation to the measurement accuracy is the distortion produced by nonlinearity in the transfer function of the encoder portion of the ADC, in terms of Integral Nonlinearity (INL) and Differential Nonlinearity (DNL). INL error introduces harmonic distortions resulting in static measurement error, which may cause problems in multiple cavity accelerators because of the interactions between cavities. DNL errors of pipelined ADCs at some particular analog input levels may be significant and result in unpredicted gains around the operating points which may degrade the dynamic performance. In LLRF system the analog input is sampled around some fixed phases and the corresponding analog input levels of each sampled data are around constant values except a transient state. Therefore DNL errors of an ADC

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around these input levels are critical to field regulation error. Currently, these measurement errors resulting from INL and DNL as reported in Analog Device Application Notes are considerable in high-speed pipelined ADCs and maybe exceed the specified precision of requirements for future accelerators, such as European X-FEL which requires an amplitude error within 0.01% and a phase error within $0.01^\circ$[9].

One way to suppress these nonlinearities is to sample analog input at more levels than four levels, $I$, $Q$, $-I$, $-Q$ in relation to IQ sampling. Larry Doolittle has introduced a non-IQ sampling method[10] in order to reduce nonlinearities and improve band-limited performance, and given an analysis and an implementation of it. His near-IQ approach is based on his previous IQ algorithm and needs ADCs to sample around IQ relationship. We extended his idea and obtained a more universal generalization of sampling method for arbitrary frequency relationship between ADC/DAC clocks and IF signal. This generalization will be presented in this paper including its analysis, implementation, simulation and comparison to conventional IQ sampling method.

First, nonlinearities of IQ sampling method are discussed in section 2. In section 3, the transfer matrices of a non-IQ algorithm are derived using state variable description. In section 4, an implementation of this non-IQ method is given and its Cross-Domain-Clock (CDC) synchronization is discussed. Then in section 5, based on particular nonlinear assumptions the advantages of the non-IQ method are compared to IQ method in simulation. finally, our conclusions are given in section 6.

## 2 The nonlinearity of IQ sampling method

High resolution data converters typically use multistage techniques to achieve high bit resolution without large comparator arrays that would be required if traditional flash ADC techniques were employed. The multistage converter typically provides more economic use of silicon. For example, the AD6645 (14 bit, 105 million samples per second) used in Storage Ring LLRF of SSRF includes a 5 bit ADC1, followed by a 5 bit ADC2 and a 6 bit ADC3. The only significant DNL errors occur at the ADC1 transition points, while the second and third stage DNL errors are minimal. There are $2^5 = 32$ decision points associated with ADC1, which occur every 68.75 mV ($2^9 = 512$ LSBs (Least Significant Bits)) for a 2.2 V full-scale input range. Compared with the linear transfer function of an ideal ADC, Fig. 1 shows an exaggerated representation of these repetitive nonlinearities of real ADC which are reported in Analog Devices application notes.

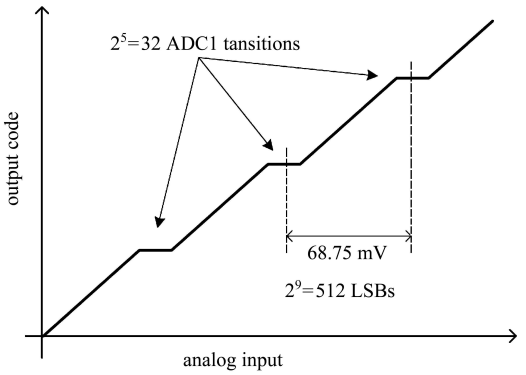


Fig. 1. Exaggerated AD6645 subranging DNL errors. Detailed information can be found in Analog Devices Application notes.

Considering the input noise to LLRF system from a cavity is very small, although the worst DNL error of ADC may be less than $\pm 0.5$ LSB (to ADC6645), the repetitive nature of the transfer function can play havoc with low level signals and add extra noise. Furthermore, in a digital LLRF control system, if the steady stead operating point is sampled at the transition point of ADC1 where there is a larger DNL error, the controller will see an unpredicted gain and the system may become unstable around the operating point. Because $I$ and $Q$ signals are orthogonal, all additional noise of $I$ and $Q$ signals directly results in cavity noise.

INL errors of ADCs introduce additional harmonic distortions which result in frequency aliasing, and lead to static deviations between real cavity fields and IQ data sampled by ADC. Since the integral part of a proportional-integral controller can reduce the steady-state error of the controller toward zero even there are nonlinear parts in the loop such as a klystron, these deviations eventually result in static errors between setting values and real cavity fields. Generally, sharp band pass filters are used to restrain harmonics to reduce aliasing nonlinearity, but which are still considerable in high precision LLRF control system. The influences of static nonlinear deviations in accelerators with multiple cavities such as SSRF are worse than those with single cavity because of the interactions between cavities.

Non-IQ sampling takes DNL errors and pushes them to frequencies where they can be digitally filtered away. In non-IQ method, an ADC samples at more analog input levels than in IQ method, and the probability of more than one data sampled at ADC transition levels is small, thus the worst DNL error can be averaged out. The static nonlinear relations between setting values and real cavity fields caused by aliasing can also be averaged out.

## 3 State variable description of a non-IQ algorithm

The relation between ADC sample period $T_{\rm S}$ and IF signal period $T_{\rm IF}$ can be written as

$$T_{\rm S}=\left(n\pm\frac{M}{N}\right)\cdot T_{\rm IF},\quad M<N\in Z\ . \tag{1}$$

Generally, $M$ is equal to 1. $n>0$ indicates down sampling, and $N$=4 means $I/Q$ relation. Theoretically, the terms $n$ and $M$ do not take any effect in reducing nonlinearities. Here we will yield the algorithm of data stream transmission from ADC clock domain to DAC clock domain on arbitrary clock relationship in terms of $N$. Generally, we consider ADC sequential samples of IF signal as discrete sinuous wave

$$a_n=|A_{\rm AD}|\cdot\cos\left(\omega T_{\rm AD}n+\phi\right), \tag{2}$$

where $|A_{\rm AD}|$, $\omega$ are the amplitude and frequency of IF signal, $\phi$ is the phase offset, and $T_{\rm AD}$ is the period of sampling clock of ADC. In IQ relation, $a_n, a_{n-1}$ are $I$ and $Q$. Mathematically, every two consecutive sample data $a_n, a_{n-1}$ carry all information (amplitude and phase) of the sinuous wave whatever the sampling clock is except half of the integer multiple of the signal frequency. We can define two state variables for ADC and DAC sample data and an imaginary orthogonal IQ reference,

$$\bar{a}_n=\begin{pmatrix}a_n\\ a_{n-1}\end{pmatrix},\bar{b}_m=\begin{pmatrix}b_m\\ b_{m-1}\end{pmatrix},\bar{r}_n=\begin{pmatrix}\cos(\omega T_{\rm AD}n)\\ \sin(\omega T_{\rm AD}n)\end{pmatrix}. \tag{3}$$

The phase shift term on $\bar{r}_n$can be written as

$$e^{{\rm i}\theta}\Leftrightarrow\begin{pmatrix}\cos\theta & -\sin\theta\\ \sin\theta & \cos\theta\end{pmatrix}. \tag{4}$$

The relationship of all above state variables is illustrated in complex plane in Fig. 2.

Now the problem is to obtain $\bar{b}_m$ from $\bar{a}_n$. The relation between $\bar{r}_n$, $\bar{a}_n$, $\bar{a}_{n-1}$, $\bar{b}_m$, $\bar{b}_{m-1}$ and $\phi$, $\theta$ can be written for matrix representation

$$\begin{cases}\bar{a}_n=|A_{\rm AD}|\cdot M\left(\omega,T_{\rm AD}\right)e^{{\rm i}\phi}\bar{r}_n=P\left(\omega,T_{\rm AD}\right)\bar{a}_{n-1}\\ \bar{b}_m=|A_{\rm DA}|\cdot M\left(\omega,T_{\rm DA}\right)e^{{\rm i}(\phi+\theta)}\bar{r}_n=P\left(\omega,T_{\rm DA}\right)\bar{b}_{m-1}\end{cases}, \tag{5}$$

where $|A_{\rm AD}|$, $|A_{\rm DA}|$ are the amplitudes of $a_n$, $b_m$. Matrices $M$, $P$ are

$$\begin{cases}M\left(\omega,T\right)=\begin{pmatrix}1 & 0\\ \cos\omega T & \sin\omega T\end{pmatrix},\\ P\left(\omega,T\right)=Me^{{\rm i}\omega T}M^{-1}=\begin{pmatrix}2\cos\omega T & -1\\ 1 & 0\end{pmatrix}.\end{cases} \tag{6}$$

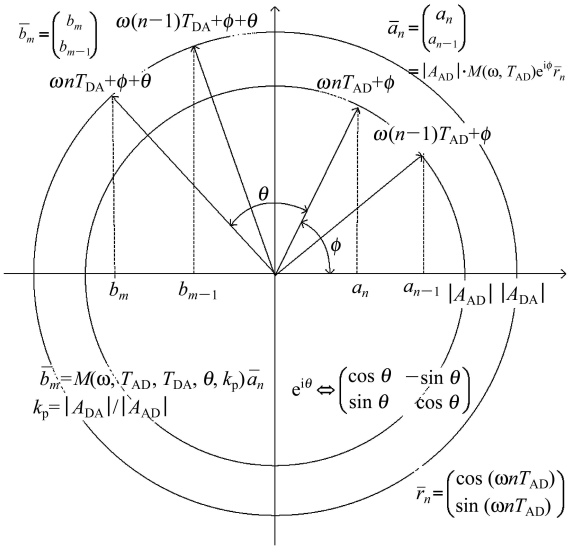


Fig. 2. Non-IQ state variable representation.

Defining $\theta$ as the phase shift, we can get the synchronizing equation for the data transmission from $\bar{a}_n$ to $\bar{b}_m$

$$\bar{b}_m=M_{\rm S}\left(\omega,T_{\rm AD},T_{\rm DA},\theta,k_{\rm p}\right)\bar{a}_n\ , \tag{7}$$

where

$$M_{\rm S}\left(\omega,T_{\rm AD},T_{\rm DA},\theta,k_{\rm p}\right)=$$
$$k_{\rm p}M\left(\omega,T_{\rm DA}\right)e^{{\rm i}\theta}M\left(\omega,T_{\rm AD}\right)^{-1}, \tag{8}$$

$k_{\rm p}=|A_{\rm DA}|/|A_{\rm AD}|$ is the proportional gain of the controller. Note that the setting values of amplitude and phase ($I$ and $Q$) still should be processed out of the above non-IQ algorithm. Assuming that the digital period of ADC is $N$, the integration part of controller can be simply accomplished by

$$H\left(z\right)=\frac{k_{\rm i}}{1-z^N}\ , \tag{9}$$

where $k_{\rm i}$ is the integral gain. This approach brings in additional poles, but doesn't damage loop stability on condition that $N$ is not very large because the bandwidth of cavity is narrow. The whole data flow is shown in Fig. 3. An implementation of the non-IQ algorithm part in Fig. 3 is described in next section.

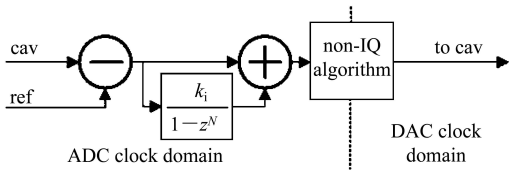


Fig. 3. Data flow with non-IQ controller.

## 4 Implementation and synchronization

Figure 4 shows a kind of logical implementation of non-IQ algorithm. At some particular time ticks,

$\bar{b}_m$ is synchronized to $\bar{a}_n$ by $M_{\rm S}$. Otherwise, $\bar{b}_m$ is automatically updated by $P(\omega, T_{\rm DA})$. Therefore, Direct Digital Synthesis (DDS) can be eliminated. The periodical synchronization also avoids possible convergence and phase slipping due to the quantization error of the auto update. The synchronization should take place every $LCM(T_{\rm AD}, T_{\rm DA})/T_{\rm DA}$ ADC clocks or every $LCM(T_{\rm AD}, T_{\rm DA})/T_{\rm AD}$ DAC clocks, at the time of their common clock edge. Here $LCM$ means the Lease-Common-Multiple.

Elements of $M_{\rm S}$ and $P(\omega, T_{\rm DA})$ which are calculated from $\omega, T_{\rm AD}, T_{\rm DA}, \theta, k_{\rm p}$ in host PC should be written to the Field Programmable Gate Array (FPGA). $\theta, k_{\rm p}$ may change during operating while $\omega, T_{\rm AD}, T_{\rm DA}$ only involve deferent clock configurations of ADC and DAC and IF frequency. A set of Matlab code has been developed to calculate these two matrices which serve both simulation and FPGA hardware. A dedicate CDC logic has been built to control the synchronization as discussed above.

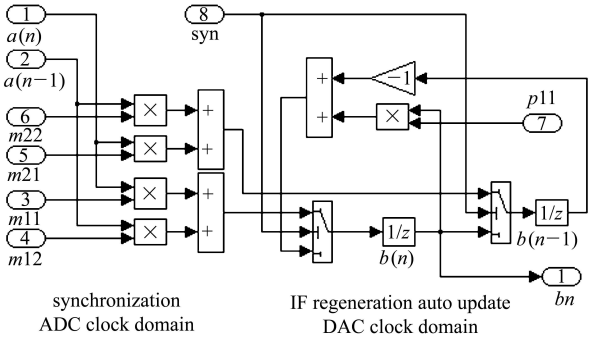


Fig. 4. A logical implementation of non-IQ algorithm.

## 5 Simulation and comparison

The DNL at particular input level introduces unpredictable gain which can be less than or more than the ideal gain as show in Fig. 5. Specifically, case (a) shows a dead zone dynamic and case (b) shows a large or infinite gain. In case (a), the gain around operating area is low so the controller can not suppress the external disturbance and add static control error. In case (b), the gain is so large that the control system can not be stable and acts like a chaos system. Both cases result in repetitive control errors.

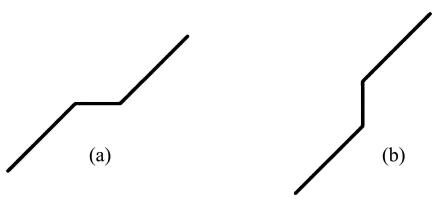


Fig. 5. Different kinds of DNL errors dead zone or small gain (a) fiction dynamic (large or infinite gain) (b).

We built a simulation loop to test the effect of non-IQ sampling method which is shown in Fig. 6 as well as a simulation result. We can see that the distortion caused by DNL error decreases as $N$ increases. Note that Fig. 6(b) is just one set of data from a lot of complicated simulation results of the nonlinear behavior around the operating point.

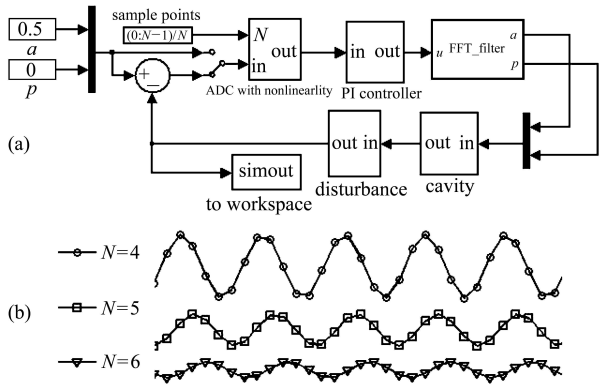


Fig. 6. (a) The simulation loop; (b) Improvement of dynamic performance as $N$ increases.

The suppression of static error with non-IQ sampling method can be simulated in an easy way. A nonlinear component which brings in harmonious can be written as

$$g_0(x) = x + a_2x^2 + a_3x^3 + a_4x^4 + a_5x^5 \ . \qquad (10)$$

Here we only consider the harmonic of order less than 6 and assume $a_2, a_3, a_4, a_5$=0.01×(1,1/2,1/4,1/8). Let a sinuous IF wave pass $g_0(x)$, then sample it and derive the base signal using FFT. The detailed steps are:

1) Let a sinuous wave pass through $g_0(x)$;

2) Sample the output signal with different $N$ values;

3) Make a FFT transform;

4) Pick up the amplitude and phase at frequency of the original IF signal;

5) Do step 1 — step 4 at deferent sample phase;

6) Plot the deviation from original IF signal at different sample phase as shown in Fig. 7.

Higher frequency simple clock yields short time delay $\tau_{\rm d}$ to the same latency of a given FPGA design. The total time delay $\tau$ consists of the analog delay $\tau_0$ and the digital delay $\tau_d$, that is $\tau = \tau_0 + \tau_{\rm d}$. The dynamic performance increases as the total time delay $\tau$ decreases. By assuming that the integral term $K_I$ cancels the pole of the cavity, the close loop transfer function can be written as

$$\Phi(s) = \frac{k_{\rm p}\omega_{\rm b}{\rm e}^{-\tau s}}{s + k_{\rm p}\omega_{\rm b}{\rm e}^{-\tau s}} \ . \qquad (11)$$

For SSRF, the bandwidth of cavity is about $\omega_{\rm b} \approx$ 1.4 kHz, $\tau_0 \approx 1$ μs, latency is about, and $k_{\rm p} \approx 50$.

The total time delay is about $\tau \approx 1+10/(38.4N)$ μs. For evaluating the dynamic performance, we can compute step response to get the setup time $t_s$ (defined within ±1% final error) and overshoot $\sigma$% of different $N$ from Eq. (11), as shown in Fig. 8.

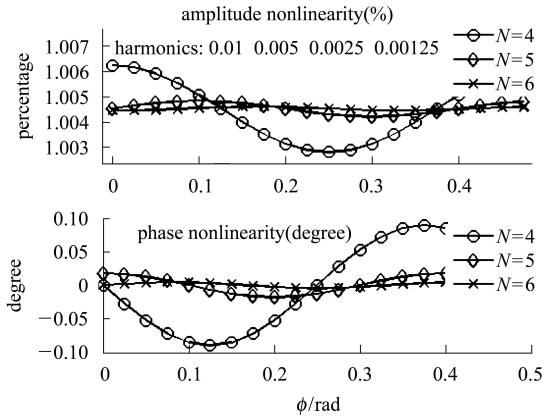


Fig. 7. Static nonlinear deviations decrease as $N$ increases (amplitude and phase). This figure shows that large $N$ averages out more nonlinearity. $N=4$ (namely $I/Q$ relation) results in the worst linearity.

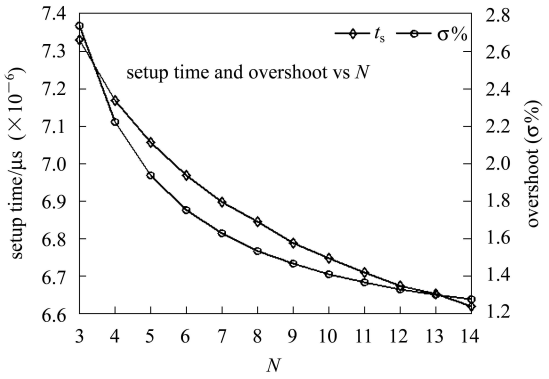


Fig. 8. Setup time and overshoot decrease as $N$ increases.

Although the majority of total time delay is analog path, we still can see from Fig. 8 that both the setup time and the overshoot decrease as $N$ increases. This indicates that the larger the $N$ is, the better the dynamic performance we can attain.

## 6 Conclusion

We developed a non-IQ PI control algorithm of digital LLRF feedback control system. The analysis, logical implementation, simulation and comparison are presented. Theoretically, this algorithm has been proven to work on arbitrary configuration of clocks, reduce nonlinearities, improve dynamic performance, and enable us to employ the highest chip speed without suffering from the $I/Q$ relation.

More detailed work in hardware should be carried out in the future. The hardware in one LLRF system of SSRF includes an Altera EP2S60 DSP board, an AD9510 PLL evaluation board, and an AD9858 DDS evaluation board. We employed a NIOS II soft processor core in EP2S60 and developed a Low-Weight Internet Protocol (LWIP) stack based on the μ C/OS-II operating system. A Labview application with EPCIS support commutates with the NIOS over TCP/IP and write/read data between the host and the FPGA. The next step is to test this non-IQ algorithm in this hardware.

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## References

1 WANG Fang, WANG Guang-Wei, LU Jian-Fa. HEP & NP, 2004, **28**(1): 88 (in Chinese)
2 WANG Fang, WANG Guang-Wei. Nuclear Techniques, 2004, **27**(1): 18 (in Chinese)
3 WANG Fang, WANG Guang-Wei, LU J F. Low Level Control RF System for SSRF, APAC, 2001. Beijing, China, 2001
4 ZHAO Yu-Bin et al. Digital Prototype of Low Level RF for SSRF, Chin. Phys. C (HEP & NP) (in press)
5 Ziomek C. Digital I/Q Demodulator, PAC 1995. SLAC-PUB-95-6857
6 Champion M, Crofford M, MA H et al. The Spallation Neutron Source Accelerator Low Level RF Control System, PAC2003. 3377—3379
7 Doolittle L, Lo C C, Monroy M, Ratti A. The SNS front end LLRF system. Proceedings of LINAC 2002. Gyeongju, Korea
8 CHEN S Y, XU H J, ZHAO Z T. PAC, 1999, **1**: 209
9 Simrock S et al. Conceptual LLRF Design for the European XFEL, LINAC 2006
10 Lawrence Doolittle, MA Heng-Jie. Mark Stuart Champion. Digital Low-Level RF Control Using Non-IQ Sampling. Proc. LINAC 2006. THP004