Calculation and Test of 150V Direct Switch Modulator Model

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Abstract In order to get some experience to build a new modulator for DESY TESLA Test Facility (TTF), a 150V direct switch long pulse modulator has been designed. Compared to the modulator solution currently used at TTF, the new proposed one has some advantages. Part of the simulation calculation of the 150V direct switch modulator is given in this paper. At the same time, a 150V modulator model was constructed and measured. The test results show that the output voltage flat-top ripple is only ± 0.53 % .

Key words direct switch modulator, storage capacitor, droop compensation circuit (DCC)

1 Introduction

The 150V direct switch modulator is mainly composed of a $30\mu F$ storage capacitor, a droop compensation circuit (DCC), two DC power supply and some semi-conductor switches (see Fig. 1). During operation the DC power supply charges the storage capacitor (C_1) voltage to 150V and the storage capacitor discharges by 5.73 % of its initial voltage in a 1.5ms pulse duration. To correct the voltage slope to less than 0.50 % , a CLC droop compensation circuit (DCC) is used. The droop compensation circuit, which is composed of a primary capacitor, a secondary capacitor and an inductor, compensates the voltage droop from the storage capacitor. The DCC primary capacitor C_3 is charged to an appropriate voltage and discharges to the secondary capacitor (C_2) through the inductor. The value of $100\mu H$ inductor is chosen, according to the simulation results. In order to get a nearly linear voltage in the 1.5ms main pulse to compensate the voltage droop from the storage capacitor, a high frequency semi-conductor switch should be used. The switch frequency must be high enough and the switch on-time will be continuously increased in the 1.5ms main pulse duration.
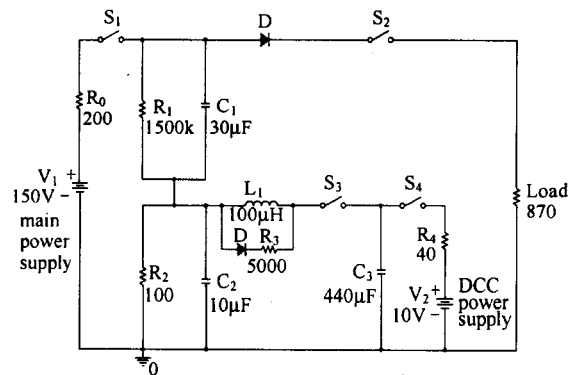

Fig.1. 150V modulator circuit (conceptual).

Compared to the modulator solution currently used at TTF, the proposed one has some advantages as following[1,2]: (1)lower storage capacitor, $30\mu F$ instead of $1400\mu F$, (2)lower droop compensation circuit inductor, $100\mu H$ instead of $330\mu H$, (3)significantly lower losses on cables, (4)no matching network, (5)no pulse transformer, (6)no filling with isolating oil necessary.

2 Simulation calculation

Summarized below are the Pspice simulation results when the DCC switch frequency is 6.67kHz, 16.67kHz and 33.33kHz in the 1.5ms main pulse duration.

2.1 DCC switch frequency $f = 6.67$kHz

During the 1.5ms pulse, the DCC switch operates 10 times, so the operation cycle is 150μs and the frequency is 6.67kHz. The shortest on-time of the DCC switch is 24μs, and the longest on-time is 80μs (Table 1).

Table 1. ($T = 150\mu s, f = 6.67$kHz).

No.	1	2	3	4	5	6	7	8	9	10
On-time/μs	24	28	30	32	34	38	42	48	60	80

Fig.2 shows the voltage waveforms of the storage capacitor (C_1) and DCC secondary capacitor (C_2) during the 1.5ms main pulse. Fig.3 shows the voltage waveform of the load. The output peak to peak voltage ripple is as
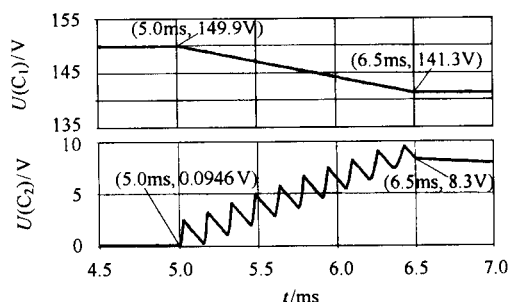

Fig.2. Voltage waveforms of the storage capacitor and DCC secondary capacitor.
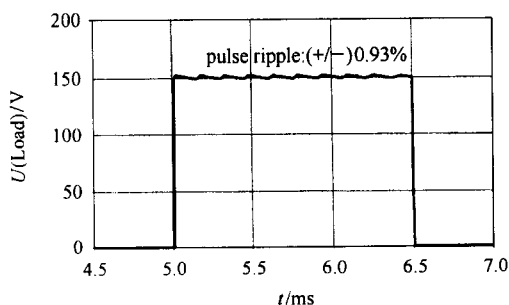

Fig.3. Voltage waveform of the load.

large as ± 0.93% due to the larger ripple voltage of the DCC secondary capacitor. So it is necessary to increase the DCC switch frequency.

2.2 DCC switch frequency $f = 16.67$kHz

During the 1.5ms pulse, the DCC switch operates 25 times, so the operation cycle is 60μs and the frequency is 16.67kHz. The shortest on-time of the DCC switch is 16μs, and the longest on-time is 60μs (Table 2). Fig.4 shows voltage waveforms of the storage capacitor (C_1) and DCC secondary capacitor (C_2) during the 1.5ms main pulse. Fig.5 shows that the output load voltage waveform ripple is about ± 0.50%.
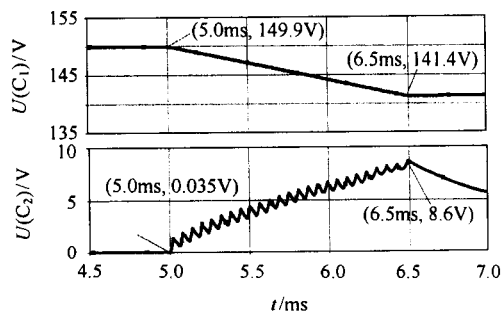

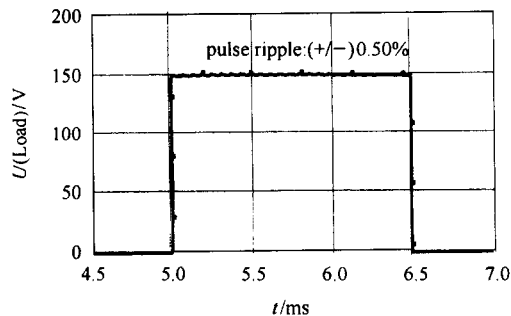Fig.4. Voltage waveforms of the storage capacitor and DCC secondary capacitor.

Fig.5. Voltage waveform of the load.

Table 2. ($T = 60\mu s, f = 16.67$kHz).

No.	1	2	3	4	5	6	7	8	9	10	11	12	13
On-time/μs	16.0	16.5	17.0	17.5	18.0	18.5	19.0	19.5	20.0	21.0	22.0	23.0	24.0
No.	14	15	16	17	18	19	20	21	22	23	24	25	
On-time/μs	25.0	26.0	27.0	28.0	29.0	31.0	33.0	36.0	41.0	45.0	49.0	60.0	

2.3 DCC switch frequency $f = 33.33$kHz

During the 1.5ms pulse, the DCC switch operates 50times, so the operation cycle is 30μs and the frequency is 33.33kHz. The shortest on-time of the DCC switch is

10μs, and the longest on-time is 30μs (Table 3). Fig.6 shows voltage waveforms of the storage capacitor (C_1) and DCC secondary capacitor (C_2) during the 1.5ms main pulse. Fig.7 shows that the output voltage waveform ripple of the load is about ± 0.33%.

Table 3.　($T = 30\mu s, f = 33.33$kHz).

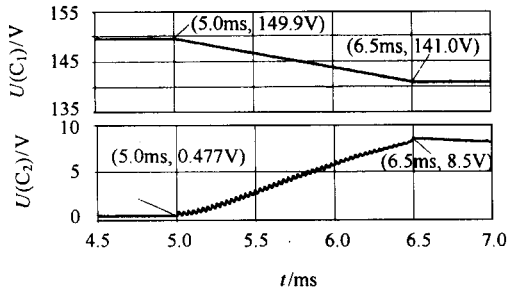| No.	1	2	3	4	5	6	7	8	9	10	11	12	13
On-time/μs	10.0	10.5	11.0	11.2	11.4	11.6	11.8	12.0	12.2	12.4	12.6	12.8	13.0
No.	14	15	16	17	18	19	20	21	22	23	24	25	26
On-time/μs	13.2	13.4	13.6	13.8	14.0	14.3	14.5	14.8	15.0	15.3	15.5	15.8	16.0
No.	27	28	29	30	31	32	33	34	35	36	37	38	39
On-time/μs	16.3	16.5	16.8	17.0	17.5	18.0	18.5	19.0	19.5	20.0	20.5	21.0	21.5
No.	40	41	42	43	44	45	46	47	48	49	50		
On-time/μs	22.0	22.5	23.0	24.0	25.0	26.0	27.0	28.0	29.0	29.8	30.0		

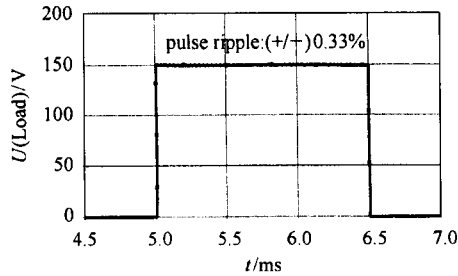Fig.6.　Voltage waveforms of the storage capacitor and DCC secondary capacitor.

Fig.7.　Voltage waveform of the load.

3　150V modulator model

In order to test the simulation results, a 150V direct switch long pulse modulator was constructed and tested[3]. According to the calculation of the droop com
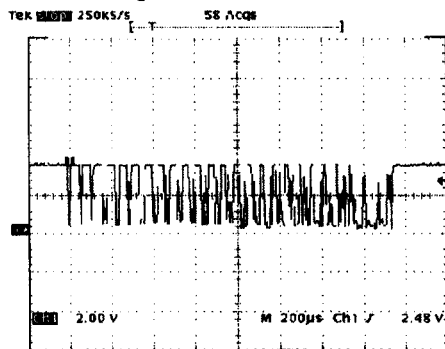

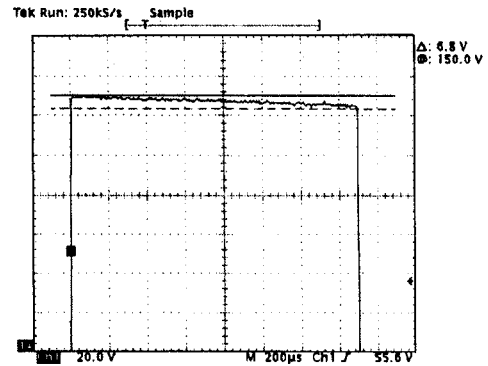Fig.8.　Test waveform of the DCC switch trigger voltage.
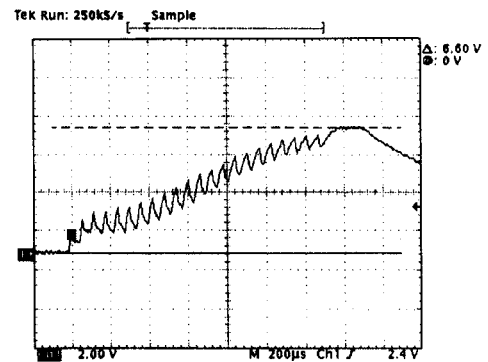

Fig.9.　Test waveform of the storage capacitor voltage.

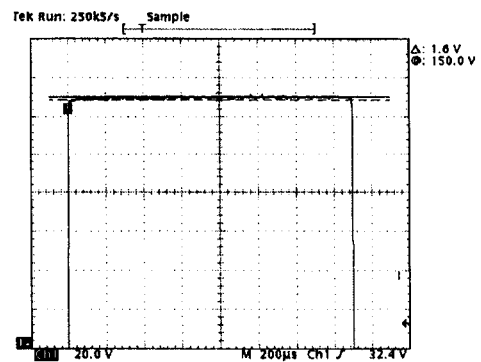Fig.10.　Test waveform of the DCC secondary capacitor voltage.

Fig.11.　Test waveform of the load voltage.

pensation circuit, 16.67kHz of DCC switch frequency is chosen. Fig.8 shows the test waveform of the DCC switch

trigger voltage. The DCC switch on-time (negative voltage in Fig. 8) is continuously increased in the 1.5ms main pulse duration.

The storage capacitor voltage, the DCC secondary capacitor voltage and the load voltage waveforms of the 150V modulator model have been measured. Fig.9 shows a test waveform, in which the storage capacitor voltage droop is 4.27 % in the 1.5ms pulse duration. Fig. 10 shows a test waveform of the DCC secondary capacitor voltage, in which the compensation capacitor voltage rises from zero to 6.6V in the 1.5ms pulse duration. Fig.11 shows the test waveform, in which the load voltage ripple is ± 0.53 % in the 1.5ms pulse duration.

4　Conclusion

The characteristics of a 150V direct switch long pulse modulator have been simulated. In order to examine the feasibility of the modulator design, a 150V direct switch modulator model has been made and tested. The test results show that the simulation calculation of the 150V modulator is reasonable.

References

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150V 直流开关调制器模型的计算和测试

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摘要　为了德国电子同步辐射加速器(DESY)的 TESLA 测试设备(TTF)研制新型调制器积累一些必要的经验,设计了一种 150V 的直流开关长脉冲调制器模型.与 TESLA 测试设备上正在使用的调制器相比,这种新的方案有许多优势.本文给出了这种调制器电路的部分模拟计算结果;同时,完成了调制器模型的建立和实验测试,测试结果显示输出电压波形的平顶抖动仅为 ± 0.53 % .

关键词　直流开关调制器　储能电容器　补偿电路(DCC)